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Tunnelling in heterojunction of n-type hydrogenated nanocrystalline silicon film with p^+-type crystal silicon

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Abstract

N-type hydrogenated nanocrystalline silicon (nc-Si:H) films were deposited by the plasma-enhanced chemical vapour deposition (PECVD) technique on p^+-type crystal silicon (c-Si) substrates; then a kind of heterojunction structure of (n)nc-Si:H/(p^+)c-Si was obtained. Both negative resistance in forward current–voltage (I–V) measurements and current staircases in reverse I–V experimental curves were observed from this heterojunction of (n)nc-Si:H/(p^+)c-Si at 77 K. It was verified by the electrical experiments that this structure is a semiconductor heterojunction tunnelling diode. The forward current was considered to be dominated by interband tunnelling, excess and thermionic emission component. Within the reverse bias ranging from around 0 to −13 V, the reverse leakage current can be attributed to minority carriers instead of majority carriers tunnelling across the depletion layer of the heterojunction. By increasing the reverse applied voltage from about −13 V to −37 V, the reverse current can be ascribed to the injection of electrons via sequent resonant tunnelling through the Si nanocrystals quantum dots into the substrate. By further increasing the reverse bias, the reverse current can be assigned to carrier avalanche multiplication within the amorphous buffer layer in the depletion region to enhance the electron resonant tunnelling in the nc-Si:H layer. The results indicate that the (n)nc-Si:H/(p^+)c-Si structure is a promising candidate for digital circuit applications.

1. Introduction

The silicon tunnelling diode has been widely studied in terms of device physics, model, fabrication technology, circuit design and applications for decades [1–3]. Recently, besides the nature of nanostructures, resonant tunnelling has also been observed in nanocrystals of silicon which was naturally embedded in amorphous matrices as the so-called natural quantum confinement (NQC) system, which produces a new way of fabricating low dimension semiconductor material with the advantages of process simplicity and low cost. Tsu *et al* [4] have observed the resonant tunnelling involving discrete quantum states within silicon nanocrystals with a-SiO_2 barriers in SiO_2/Si diodes at room temperature. Burr *et al* [5] have investigated the carrier conduction in porous nanosilicon light emitting devices, of which the carrier transport is controlled by space-charge-limited currents or carrier tunnelling through potential barriers. Hastas *et al* [6] reported the heterojunction structure of nanocrystalline carbon with crystal silicon (nc-SiC/c-Si) and analysed the current

Table 1. The process parameters for fabricating the (n)nc-Si:H/(p^+)c-Si samples.

Sample	Substrate carrier concentration (cm^{-3})	$C_p = PH_3/SiH_4$ (% in volume)	RF power density (W cm^{-2})	Substrate temperature (K)	Negative dc bias (V)	Reactant pressure (Pa)
1	(p^+)c-Si 1.34×10^{19}	0.20 ± 0.05	0.6 ± 0.05	523 ± 1	-200 ± 2	100 ± 5
2	(p^+)c-Si 1.34×10^{19}	0.50 ± 0.05	0.6 ± 0.05	523 ± 1	-200 ± 2	100 ± 5
3	(p^+)c-Si 1.34×10^{19}	1.00 ± 0.10	0.6 ± 0.05	523 ± 1	-200 ± 2	100 ± 5

conduction mechanism. Weaver *et al* [7] reported the defect effect on the peak current density (PCD) and peak to valley current ratio (PVCR) of Si-based interband tunnelling diodes. The hydrogenated nanocrystalline silicon (nc-Si:H) film that comprises silicon nanocrystals embedded in a hydrogenated amorphous silicon (a-Si:H) tissue has attracted a great deal of attention due to its potential for micro-electronic devices and photovoltaic applications as well as the interesting physical properties that result from its heterogeneous nature. In our previous work [8, 9], nc-Si:H/c-Si diodes were prepared and the current staircases in reverse *I–V* curves due to carrier resonant tunnelling observed, although the negative resistance in the forward *I–V* curve was not detected.

In order to further analyse the carrier transport behaviour in nc-Si:H/c-Si, in the present work, n-type nc-Si:H films were deposited by the plasma-enhanced chemical vapour deposition (PECVD) technique on p^+-type crystal silicon (c-Si) substrates; then the structure of the electrode/(n)nc-Si:H/(p^+)c-Si/electrode was fabricated. Comparing with our previous structure [8], the depletion layer should mainly exist at the nc-Si:H side and the barrier height was decreased since a p^+ type c-Si wafer was used as a substrate. Thereby, interband tunnelling was expected to appear. In addition, an incubation layer can be introduced into the interface of the film/substrate by the PECVD film. Luckily, from the high-resolution transmission electronic microscope (HRTEM) photo of the (n)nc-Si:H/(p^+)c-Si cross section, an amorphous buffer layer of about 10 nm thickness was found in our present device. The buffer layer can be considered as a large series resistance. Further, the layer can share the majority of the reverse bias voltage and reduce the potential across the nc-Si:H layer containing the nanocrystals. Consequently, the negative applied voltage corresponding to the first current staircase in reverse *I–V* curves and the breakdown voltage of the device should be increased. Based on the analysis of the electrical measurements such as *I–V* characteristics, capacitance–voltage (*C–V*) profiling, capacitance–frequency (*C–f*) curve, deep level transient Fourier spectrum (DLTFS) and dc conductance measurement, a tunnel diode of the electrode/(n)nc-Si:H/(p^+)c-Si/electrode was demonstrated while the conduction mechanisms were investigated, as well as the crucial role of the buffer layer was analysed.

2. Sample preparation and measurement

A single facet polished p^+-type crystal silicon (1 1 1) wafer of around 100 μm thickness with an average resistivity of about 5.5×10^{-3} Ω cm ($N_A \geqslant 1.34 \times 10^{19}$ cm^{-3}) was adopted as the substrate material. The (n)nc-Si:H/(p^+)c-Si structure was prepared with a planar process. Firstly, around 100 nm thick SiO_2 layer was prepared by thermal oxidation of the substrate wafer at 1020 °C. Then, the SiO_2 layer was etched and patterned by photolithography to make an array of square holes (30 μm × 30 μm). Secondly, after an appropriate treatment, fresh n-type nc-Si:H films with different ratios of phosphine PH_3 doping in silane (PH_3/SiH_4 in volume percentage, i.e., PH_3/SiH_4 vol.%) were separately deposited on the array configuration. Then, the outer layer of the nc-Si:H film in the square holes was removed by etching and photolithography, leaving only around 50 nm thick phosphorus-doped nc-Si:H layers in the hole bottoms. The deposition process was operated in a capacitively coupled radio-frequency (RF of 13.56 MHz) PECVD system aided with direct current (dc) bias stimulation. It is worth specially emphasizing that the strongly hydrogen diluted silane, SiH_4 diluted to 1.00 vol.% in H_2, was used as a reactant source gas. Phosphine was added to the mixed reactant gas to realize doping. The process parameters are illustrated in table 1. Subsequently, Au/Cr and Au/Ge alloys as Ohmic contact electrodes were prepared by electron-beam evaporation on the side of the substrate and nc-Si:H film, respectively. The schematic structure of the electrode/(n)nc-Si:H/(p^+)c-Si/electrode is depicted in figure 1. For the convenience of electric measurements, finally the structures of the electrode/(n)nc-Si:H/(p^+)c-Si/electrode were sealed in a ceramic shell with a metal contact pad.

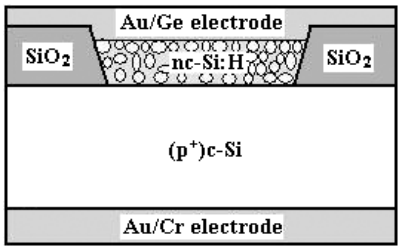

Figure 1. The schematic structure of electrode/(n)nc-Si:H/(p^+)c-Si/electrode.

The surface morphology of phosphorus-doped nc-Si:H samples was checked by scanning electron microscopy (SEM, JEM-6700F, made in Japan with an operational voltage of 10 kV) and the SEM images are presented in figures 2(*a*)–(*c*), from which one can find that the mean size of particles is independent of doping. The HRTEM photo for the cross section of (n)nc-Si:H/(p^+)c-Si was taken by a transmission electronic microscope (JEM-2010, made in Japan with an operational voltage of 200 kV and a resolution of 0.19 nm), as shown in figure 2(*d*). From the TEM photo one can detect that an amorphous buffer layer of some 10 nm thickness was incubated upon the substrate, and the nanocrystals with a size of 3–8 nm were naturally embedded in the amorphous tissues.

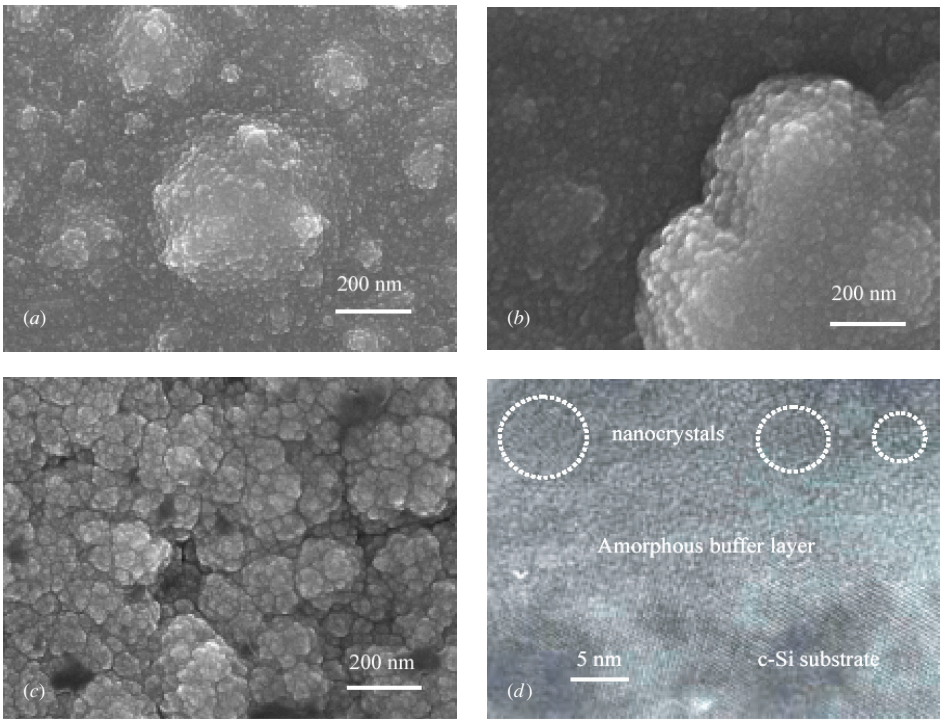

Figure 2. SEM images of nc-Si:H samples with different doping ratios: (*a*) for the sample with $C_p = PH_3/SiH_4$ vol.% = 0.20 vol.%, (*b*) for the sample with $C_p = PH_3/SiH_4$ vol.% = 0.50 vol.% and (*c*) for the sample with $C_p = PH_3/SiH_4$ vol% = 1.00 vol%. The mean size of particles depicted from the surface morphology does not change with the doping ratio. (*d*) The transmission electronic microscope (TEM) photo of the cross section of (n)nc-Si:H/(p^+)c-Si. Dashed circles indicate nanocrystals. A buffer layer of around 10 nm thickness is incubated on the c-Si substrate.

Using a HP4280A precision LCR meter, the *C–V* curves of the fabricated structure were measured by means of a dc-biased small ac signal (5 mV) of 1 MHz applied to the electrodes at 77 K, as demonstrated in figure 3(*a*). The *C–f* curves were obtained by a set of multi-frequency LCR meters (HP4274A combination with HP4275A) with a small ac signal (5 mV) from 100 to 10 MHz at 77 K, as shown in figure 3(*b*).

Testing of deep level transient Fourier spectrum (DLTFS) with temperature sweeping from 77 to 400 K was performed by a high sensitivity deep level transient Fourier spectrometer (BIO-RAD-DL8000) at different reverse biases and 0.0 V fixed pulse. The spectra of sample 1 are shown in figure 4 and the DLTFS results of all samples are presented in table 2.

To probe the current path among the nanocrystals, the dark dc conductance of the phosphorus-doped nc-Si:H film, which was grown on glass under the same prepared conditions as the (n)nc-Si:H/(p^+)c-Si sample 1, was measured using a computer-controlled Keithley 2400 sourcemeter with an Oxford Optistat$^{CF\text{-}V}$ cryostat system within the temperature range from 77 to 300 K, as shown in figure 5. The *I–V* characteristics of (n)nc-Si:H/(p^+)c-Si were conducted by a computer-controlled system including a HP4140B (PA meter/dc voltage source) at 77 K in figure 6.

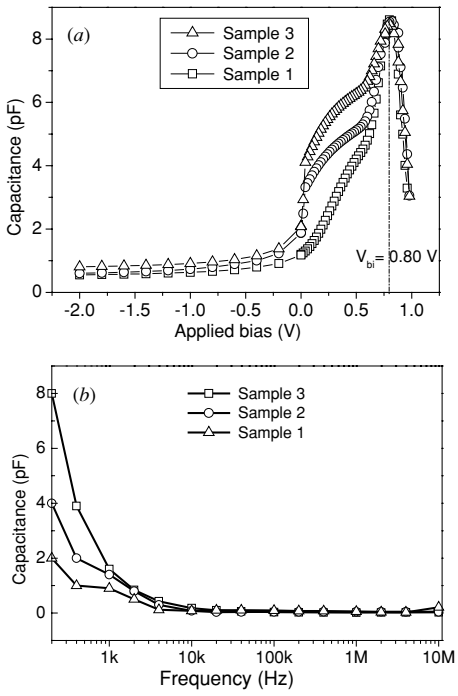

Figure 3. (*a*) Capacitance–voltage (*C–V*) characteristics and (*b*) capacitance–frequency relation (*C–f*) of the structure of (n)nc-Si:H/(p^+)c-Si at 77 K. The dots are experimental data and the connecting lines are guides for the eye.

3. Results and discussion

3.1. C–V characteristics

One can easily find from the *C–V* curves in figure 3(*a*) that the capacitance, *C*, dramatically varies with the forward applied voltage when the voltage is smaller than the built-in potential V_{bi}. Also, from the figure one can infer that

Table 2. The deep level transient Fourier spectrum (DLTFS) results of all three samples at different reverse applied biases.

Sample	V_R (V)	$(N_A - N_D)$ (10^{19} cm^{-3})	Trap level location E_T (eV)	Capture cross section Σ (10^{-15} cm^{-2})	Trap concentration N_T (10^{12} cm^{-3})	$(N_T/(N_A - N_D))$ (%)
1	−0.5	1.34	$E_1 = -0.53$	3.0	8.11	10^{-7}–10^{-6}
	−1.0		$E_1 = -0.53$	3.0	28.8	
	−2.0		$E_1 = -0.53$	3.0	70.9	
2	−0.5	1.34	$E_1 = -0.57$	3.6	45.1	10^{-6}–10^{-5}
	−1.0		$E_1 = -0.57$	3.6	71.4	
	−2.0		$E_1 = -0.57$	3.6	149.0	
3	−0.5	1.34	$E_1 = -0.61$	4.0	51.3	10^{-6}–10^{-5}
	−1.0		$E_1 = -0.61$	4.0	81.9	
	−2.0		$E_1 = -0.61$	4.0	154.4	

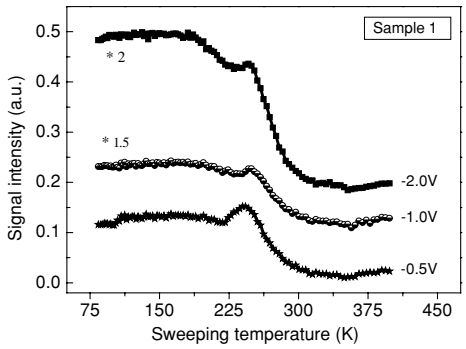

Figure 4. The deep level transient Fourier spectrum (DLTFS) of the heterojunction of (n)nc-Si:H/(p$^+$)c-Si of sample 1.

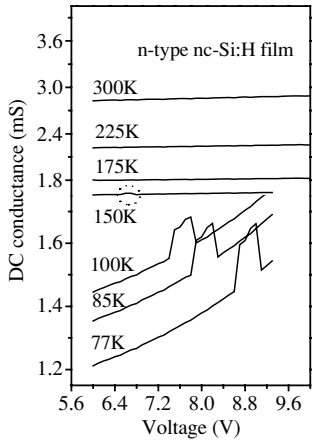

Figure 5. The dark dc conductance of the phosphorus doped nc-Si:H film ($C_p = PH_3/SiH_4\% = 0.20$ vol.%).

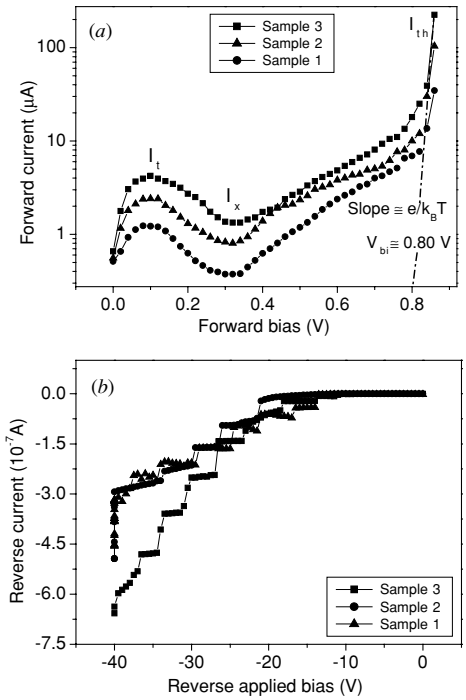

Figure 6. The current–voltage (I–V) characteristics for the structure of (n)nc-Si:H/(p$^+$)c-Si. (*a*) The forward I–V experimental curves. Within the range I increases dramatically with increasing positive applied voltage V, for sample 3, the slope of fitting tangent close to e/k_BT and the built-in potential, $V_{bi} \cong 0.8$ V. (*b*) The reverse I–V measurement plots: the dots are experimental data and the connecting lines are guides for the eye.

the structures of the electrode/(n)nc-Si:H/(p$^+$)c-Si/electrode are the single semiconductor/semiconductor heterojunction, since no peak appears in the curves at zero applied voltage [9]. Simultaneously, it can be implied from the shape transition in the C–V curves that the defect trap density in the heterojunction structure increases with increasing doping ratio since the slope for the C–f curve decreases with increasing doping ratio [10]. This result coincides with the DLTFS results in table 2, from which one can find that the trap concentration increases while the trap level falls from the bottom of the conduction band with increasing doping due to the doping induced disorder, which is mainly located in a-Si:H tissues. The result indicates that the trap belongs to the bulk defect in the nc-Si:H layer in the heterojunction [11]. In addition, one can conclude from the DLTFS results that only a few dopant atoms form the nonradiative deep traps, since both the trap concentration N_T and the ratio of N_T to net carrier concentration $N_A - N_D$, i.e., $(N_T/(N_A - N_D))$ (%), are very small.

The dependence of the barrier capacitance C on the effective charge density $\rho(\varepsilon_b)$ in the heterojunction can be expressed as [12]

$$C = kk_0\rho(\varepsilon_s) \Big/ \left(2kk_0 \int_0^{\varepsilon_s} \rho(\varepsilon)\, \mathrm{d}\varepsilon\right)^{1/2}, \qquad (1)$$

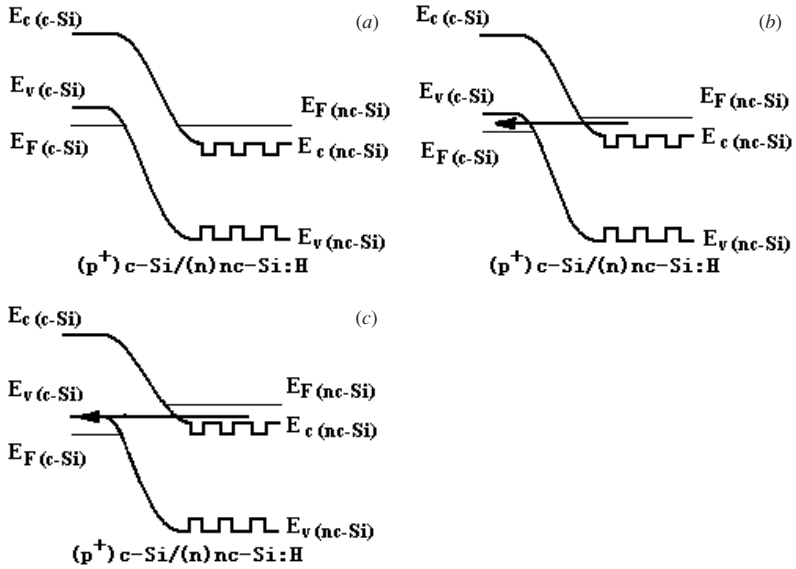

Figure 7. Energy band diagram for varying bias conditions in the heterojunction of (p$^+$)c-Si/(n)nc-Si:H. (*a*) For thermal equilibrium, zero bias, (*b*) for the situation of forward bias, applied voltage V is near V_p, I_t is up to I_p and (*c*) for the situation of forward bias, applied voltage V is near V_v; I_t is down to I_x.

where k is the relative dielectric constant of bulk silicon and k_0 is the vacuum permittivity, ε_s is the total barrier height. Expression (1) can be adopted to interpret our measurements. As we know, only the trap states whose occupation can be changed within the emission time $\tau \leqslant 1/f$ (f for the excited signal frequency) can contribute to $\rho(\varepsilon_b)$, namely, to the barrier capacitance C. Accordingly, the barrier capacitance C decreases with increasing excited signal frequency f, as shown in figure 3(*b*). On the other hand, from the DLTFS results shown in table 2, the fact that the trap concentration N_T increases with increasing doping can induce that C increases with increasing doping ratio according to formula (1), which is demonstrated in figure 3(*a*). Therefore, the deeper the trap is located, the faster the capacitance drops with increasing excited signal frequency, as shown in figure 3(*b*).

3.2. Coulomb-blockade effect

It is worth noting that the shoulders in C–V curves should be attributed to electron trapping in the embedded nanocrystal quantum dots rather than the hole one from the Coulomb-blockade effect [10]. According to the dark dc conductance (G) measurement for a phosphorus-doped nc-Si:H film, the fact that apparent peaks emerge in G–V curves as presented in figure 5, reveals the Coulomb-blockade behaviour below 150 K. A peak appears near a bias of 6.6 V at 150 K and towards a higher voltage with the decreasing temperature until reaching 8.7 V at 77 K. Generally speaking, in thin films containing nanograins, such current peaks could be detectable only if (i) there is a well-defined current path amongst the nanograins and (ii) the nanograins are well ordered. Furthermore, according to the condition of emerging the Coulomb-blockade effect [4, 13]:

$$C < \frac{e^2}{2K_B T}, \tag{2}$$

where C is the single quantum dot capacitance, e is the electron charge and k_B is the Boltzmann constant. For our case, the capacitance C is estimated to be smaller than 6.18×10^{-18} F.

Here the capacitance for a nanocrystalline silicon quantum dot is not the same as the classical case due to discrete electrons in the Coulomb-blockade phenomenon. One needs to consider that the dielectric constant in nanocrystalline Si is different from that of the a-Si:H matrix where the quantum dot is embedded. Also, taking into account the quantum size effect, the relative dielectric constant ε_r of nanocrystalline Si is smaller than that of bulk silicon. Thus, in the case of bringing an electron to quantum dot, Tsu defines the quantum dot capacitance C as [14]

$$E^Q_{n+1} - E^Q_n = \frac{e^2}{2C^Q_{n+1}}, \tag{3}$$

where $E^Q_{n+1} - E^Q_n$ is the Coulomb-blockade energy, Q refers to the quantum mechanics method, n is limited to $n = 0$ and $n = 1$ because of the use of perturbation calculations. The value of nanocrystalline silicon capacitance of 6.18×10^{-18} F in the present structure is in coincidence with the capacitance C^Q_1 of a 8 nm sized quantum dot in the case of $n = 0$ by quantum mechanics calculation in [14]. Thereby, the Coulomb-blockade energy $E^Q_{n+1} - E^Q_n$ for the nanocrystal silicon can be calculated as about 13 meV according to expression (3) with $C = 6.18 \times 10^{-18}$ F in the present device. It is as significant as the value from Tsu in the nanocrystal silicon size of 3.0 nm [4]. The error between our result and Tsu's can be presumed to derive from the difference on the matrix where the quantum dot is embedded. Therefore, the Coulomb-blockade effect can be considered to play an important role in the resonant tunnelling conduction for our devices.

3.3. Forward I–V characteristics

When the applied bias voltage of the (n)nc-Si:H/(p$^\pm$)c-Si structures is zero, the heterojunction is in thermal equilibrium, as shown in figure 7(*a*); the current is zero.

By increasing the low positive voltage applied to the (n)nc-Si:H/(p$^+$)c-Si samples, the current formed is the so-called interband tunnelling current I_t [1]. The current I_t continues to increase up to the largest peak value I_p at the peak voltage V_p, as indicated in figure 6(*a*). It can be assigned to the occupied states on the n-type nc-Si:H side coinciding with the empty allowed states on the p$^{\pm}$ c-Si side as the positive bias voltage increases, as displayed in figure 7(*b*). Subsequently, by further increasing the positive applied voltage, the conduction band on the (n)nc-Si:H side becomes uncrossed with the valence band on the (p$^+$)c-Si side; the current I_t decreases to the smallest valley value I_v while the negative resistance can be clearly observed at 77 K, as illustrated in figure 6(*a*). It can be due to the lack of allowed states of corresponding energies for tunnelling, as represented in figure 7(*c*). The tunnelling current I_t can be expressed as [15]

$$I_t = I_p(V/V_p)\exp(1 - V/V_p), \tag{4}$$

where I_p is the peak current and V_p is the peak voltage value corresponding to I_p. The current I_t falls to the residual component by increasing the positive applied voltage up to the valley voltage V_v. The residual current is the so-called excess current I_x, which is considered to be mainly dominated by the electron multistep tunnelling from the conduction band via localized gap states in the forbidden band gap to the valence band [6, 7, 16]. As one can see from the DLTFS measurement, the trap state density increases with increasing doping ratio; it will result in the enhancement of the multistep tunnelling probability. Accordingly, the excess current I_x will increase with increasing doping ratio on the nc-Si:H side. It is just the result in figure 6(*a*). The current I_t can be described as [17]

$$I_x = I_v \exp(A'(V - V_v)), \tag{5}$$

where V_v is the valley voltage and A' is the coefficient.

When the positive applied bias is higher than the valley voltage V_v, the measured current I value increases exponentially with increasing applied voltage V, which indicates that the normal diffusion (or thermal) current will be governed as in the case of usual p–n junction semiconductor diode. Using a computer program, the least-squares fitting of I–V experimental data for one sample (within the range of I dramatically increasing with V) was performed. Accordingly, the slope of fitting tangent close to e/k_BT and the built-in potential, $V_{bi} \cong 0.8$V, were obtained, as displayed in figure 6(*a*). It is obvious that the experimental I–V curves (above the valley voltage) can be simulated by the classical junction rectification model as the empirical relationship [15]:

$$I_{th} = I_0 \exp(AV - 1), \tag{6}$$

where I_0 is the saturation current and A is the coefficient. This component comes from the carrier thermionic emission as the so-called thermal current I_{th}. Thus, the total forward current can be given as follows:

$$I = I_t + I_x + I_{th}. \tag{7}$$

The ratio of the peak current to the valley one (PVCR), I_p/I_v, shows little dependence on the variation of doping on the nc-Si:H side, as plotted in figure 6(*a*). It can be interpreted as follows. On the one hand, the tunnelling peak current enhances with the decrease of the heterojunction barrier height and the depletion layer width, due to the increase in the carrier concentration from doping in the nc-Si:H layer. On the other hand, the excess current increases with the gap state density originating from doping. Thus the ratio of I_p/I_v does weakly vary with doping. As a result, the relative steady PVCR in the present structures does show a difference from that of Si-based interband tunnelling diodes from other researcher groups [7], the change of PVCR in the latter derived from altering the quantum well size and disorder.

3.4. Reverse I–V characteristics

As shown in figure 6(*b*), by increasing the negative applied voltage from about 0 to −13 V, the reverse leakage current I_r is just the order of magnitude of 10^{-10} A, and does weakly depend on the electrical field at 77 K. The conduction behaviour within this negative applied voltage range is dominated by tunnelling instead of electrical field-enhanced electron emission [15]. It can be comprehended according to the DLTFS results. As demonstrated in table 2 and figure 4, the trap concentration N_T and the measured signal intensity increase with enhancing the bias voltage V_R, which indicates that N_T increases with the depth at the nc-Si:H side from the interface of nc-Si:H/c-Si [18, 19]. The traps act as discrete bulk traps rather than continuously interface ones, since the measured signal peaks fix at a temperature and are irrespective of the reverse bias V_r, as depicted in figure 4. Thereby, a few localized states coming from the discrete bulk traps participate in the conducting processes. As a result, the little cumulative leakage current increases with increasing reverse bias. Consequently, one can deduce that the carrier transport within this negative applied voltage range is dominated by tunnelling transport, namely, the minority carriers tunnel across the depletion layer in the space charge region rather than the majority carriers.

However, within higher reverse bias ranging from about −13 to −37 V, the plots of I_r versus V_r demonstrate current staircases in figure 6(*b*). The result indicates that the current is generated from electron resonant tunnelling through the silicon nanocrystals at 77 K [4, 13]. The resonant tunnelling behaviour can be comprehended as follows. In the present structure, an amorphous buffer layer is sandwiched between the p-type heavily doped substrate and the n-type nc-Si:H layer. By increasing the negative applied voltage on the (n)nc-Si:H/(p$^+$)c-Si heterojunction, a majority of the potential drop can be assumed to take place across the high resistance amorphous layer and a minority appears across the nc-Si:H layer, while the potential drop across the (p$^+$)c-Si substrate can be neglected. As one can find from the TEM photo for the cross section of (n)nc-Si:H/(p$^+$)c-Si, the silicon nanocrystals array along the depletion direction in the nc-Si:H layer and distribute parallel to the (n)nc-Si:H/(p$^+$)c-Si interface simultaneously. The quantized energy bands can be formed in these nanocrystals as quantum dots due to the quantum size effect [4, 13], as shown in figure 8. Consequently, as the Fermi energy level in the alloy

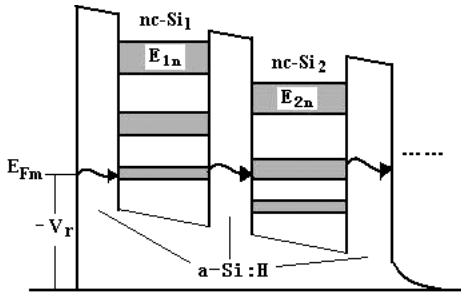

Figure 8. The schematic diagram of a grain array including two quantum dots. The shaded regions represent the quantized energy bands. E_{Fm} is the Fermi level of the Au/Ge electrode at the side of (n)nc-Si:H, $-V_b$ is the negative bias.

electrode is swept by an applied voltage past a quantum state in the nanocrystal, its energy level is shifted by a voltage that is shared by a nanocrystal capacitor. Once the condition for the Fermi energy level in the alloy electrode alignment with the *n*th quantum state in the nanocrystal is satisfied, the current jump which originated from injection of electrons via resonant tunnelling through the nanocrystal silicon quantum dot into the substrate would be observed. Accordingly, the current is mainly determined by a tunnelling component. Furthermore, in our present structure, only a few nanocrystals are involved in multi-barrier sequent resonant tunnelling [4, 8]. These different nanocrystals would generate a few different current staircases, as presented in figure 6(*b*). Otherwise, the presented current staircases corresponding to quantized energy bands can be directly related to the negative applied voltage [4, 13]. As a result, the negative applied voltage corresponding to the first current staircase decreasing with the increase of doping can be attributed to the reducing of barrier height, as indicated in figure 6(*b*). From the SEM pictures in figures 2(*a*)–(*c*), the mean size of nanocrystals does not change with the variation of doping, which indicates that the quantized energy levels in nanocrystals in different heterojunctions would be almost the same [4]. As a consequence, the number of reverse current staircases and the order of the magnitude of the reverse current are almost the same in different heterojunction samples, as shown in figure 6(*b*).

As the negative applied voltage is increased beyond −37 V, the reverse current increases sharply as displayed in figure 6(*b*). The current can be assigned to carrier avalanche multiplication in the amorphous buffer layer in the depletion region enhancing the electron resonant tunnelling in the nc-Si:H layer. As noted above, the major potential drop appears across the amorphous layer; it is likely to be broken down by the carrier avalanche multiplication when the reverse bias exceeds −37 V in the present devices. The avalanche current superposes the resonant tunnelling one so as to enshroud the current steps. Our published work on a similar structure without any buffer layer focused on the *I–V* characteristics from around −7.0 to −9.0 V. It is nearly within the applied voltage range where the Coulomb-blockade effect emerges, as presented in figure 5. However, the structure with a higher threshold voltage in the present work is sandwiched by an amorphous buffer layer. This layer can share the major reverse bias voltage while reducing the potential drop across the nc-Si:H film. As a result, the negative applied voltage corresponding to the first current staircase is increased. It should be pointed out that our present results do not contradict the former [8].

4. Conclusion

A kind of heterojunction of (n)nc-Si:H/(p^+)c-Si was fabricated. It was verified by negative resistance emerging in forward *I–V* measurement plots while current staircases appear in reverse *I–V* experimental curves at 77 K that the resulting structure is a tunnelling diode. The conduction mechanism was investigated as follows. The forward current can be ascribed to interband tunnelling, excess and thermionic emission. However, within the reverse bias ranging from around 0 to −13 V, the low reverse leakage current can be attributed to minority carrier tunnelling across the depletion layer in the heterojunction. By increasing the reverse applied voltage from about −13 V to −37 V, the reverse current can be assigned to the injection of electrons via sequent resonant tunnelling through the Si nanocrystal quantum dots into the substrate. By further increasing the negative applied voltage beyond −37 V, the reverse current can be considered as carrier avalanche multiplication enhancing the electron resonant tunnelling.

The results show that the (n)nc-Si:H/(p^+)c-Si tunnel diode is a promising candidate for digital circuit applications in the future.

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