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RESEARCH ARTICLE

Development of back-junction back-contact silicon solar cells based on industrial processes

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ABSTRACT

We have presented simplified industrial processes to fabricate high performance back-junction back-contact (BJBC) silicon solar cells. Good optical surface structures (solar averaged reflectance 2.5%) and high implied open-circuit voltage (0.695 V) have been realized in the BJBC cell precursors through wet chemical processing, co-diffusion, P ion implantation and annealing oxidation, as well as laser patterning and plasma enhanced chemical vapour deposition passivation processes. We have achieved a certified high efficiency of close to 22% on BJBC silicon solar cells with the size of 4.04 cm^2 by using screen printing and co-firing technologies. The manufacturing process flow further successfully yields efficiency of around 21% BJBC silicon solar cells with enlarged sizes of 6 × 6 cm^2. The present work has demonstrated that the commercialization of low-cost and high-efficiency BJBC solar cells is possible because we have used processes compatible with existing production lines. Copyright © 2017 John Wiley & Sons, Ltd.

KEYWORDS

silicon solar cells; BJBC; industrial processes; high performance

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1. INTRODUCTION

High-efficiency back-junction back-contact (BJBC) silicon solar cells [1–3] have always attracted extensive investigation due to their characteristic configuration in which the cells have no metal fingers and bus bars on the front side and the optical shading losses are avoided completely. The absence of the front metal contacts allows the sunward and the back side surfaces to be independently optimized for optical and electrical performance, respectively [4,5]. The most successful approach in mass production for large-area (125 × 125 mm^2) BJBC, i.e., interdigitated back contact (IBC), silicon solar cells has been realized by SunPower Corporation with cell efficiencies of 25% on high-quality n-type monocrystalline wafers [6]. Other laboratories and research institutions have also achieved progresses on small size (4 cm^2) BJBC silicon cells, e.g., the efficiency of 23.0% at Fraunhofer ISE [7], 23.1% at Institut für Solarenergieforschung [8], 23.3% at IMEC [9] and 24.4 ± 0.7% at Trina solar/Australian National University [10]. For the large-area BJBC silicon solar cells, Bosch [11] and Samsung [12] have demonstrated efficiencies of 22.1% (156 × 156 mm^2) and 22.4% (125 × 125 mm^2), respectively, with the ion-implantation technology. Trina solar has realized the efficiency of 23.5% on the 156 × 156 mm^2 Cz substrates based on screen-printed technology in 2016 [13], Panasonic has created a silicon solar cell world record of 25.6% efficiency (size 143.7 cm^2) based on combination of the BJBC structure and heterojunction technology in 2014 [14] and Kaneka Corporation has developed the new silicon solar cell top efficiencies of 24.91% (size 239.0 cm^2) [15] and 26.33% (size 180 cm^2) with the heterojunction IBC technology in 2016 [16].

Research and development of low-cost and high-efficiency BJBC silicon solar cells is an immediate task for research institutions from all over the world, in order to avoid using complex processes (e.g., photolithography and vacuum evaporation technologies) in the present mass production. Recently, some industrial relevant processed BJBC silicon cells have been reported. Zin *et al.* [17]

proposed a novel simplified technique of simultaneous etch-back to create light (n and p) and localized heavy (n^+ and p^+) diffusions. The deduced total saturation current density J_0 is below 30 fA/cm^2 by applying the etch-back technique. Yang *et al*. [18] put forward a new method consisting of patterned boron (B)/phosphorus (P) ion implantation, laser annealing and a subsequent low-temperature oxidation, and obtained a potential efficiency higher than 23% according to simulations with the experimental parameters. Hendrichs *et al*. [19] investigated three different screen-printed metallization concepts for BJBC silicon solar cells with an edge length of 156 mm. They qualified the individual loss mechanisms of each metallization concept and the maximum solar cell conversion efficiency of 22.0% by means of numerical simulations. Chen *et al*. [20] presented a methodology of using e-beam evaporation and screen printing resist to fabricate an Al-contacted BJBC silicon solar cell with efficiency of 22.72% (4 cm^2). Dahlinger *et al*. [21] fabricated the laser processed (two pulsed green laser doping and two pulsed UV laser ablation steps) BJBC silicon solar cells with efficiencies of 23.2% (4 cm^2) by the help of four novel high flexibility and spatial resolution laser irradiation processes.

One of the main challenges of BJBC silicon solar cells lies in the formation and integration in the three different doping concentration areas, i.e., the front side field (n^+ FSF), the back side field (n^+ BSF) and the emitter junction (p^+ emitter). Several diffusion steps with high process temperatures have to be carried out, resulting in an increase in the process costs. The implementation of patterning technologies (e.g., photolithography) in the process sequence leads to a further increase in the process effort. In this work, we have proposed a much simplified method based on one single high-temperature treatment (so-called co-diffusion) to form the n^+ FSF and p^+ emitter, and the P ion implantation and annealing oxidation to form the n^+ BSF after the laser patterning, together with the height difference between adjacent n^+- and p^+-doped areas on the back side (i.e., there is no need to implement the gap process). We have employed the conventional SiN_x:H antireflection coating (ARC) to passivate the front and back surfaces in combination with the screen printing and a co-firing step to sinter the different metallization pastes and to form electrical contacts for the back p^+ emitter and n^+ BSF. The best produced BJBC silicon solar cell (4.04 cm^2) has been independently confirmed with the efficiency of 22.20% by Solar Energy Research Institute of Singapore (SERIS). We have further shown the potential of the same industrial processes for large size (6 × 6 cm^2) BJBC silicon solar cells with the in-house measured efficiency up to 21.43%.

2. EXPERIMENTAL DETAILS

2.1. Solar cell preparation

Figure 1 shows the process sequences and structures for fabricating the BJBC solar cells featuring three indispensible process steps (co-diffusion to form the n^+ FSF and p^+ emitter, ion implantation and annealing oxidation to form the n^+ BSF after the laser pattern, as well as screen printing and co-firing to form the electrical contacts on the back side). As a starting material, we used (100)-oriented n-type Cz silicon wafers (156 × 156 mm^2) with a thickness of 180 μm and a resistivity of 3–4 Ω cm. After damage etching of ~10 μm/side, the wafers underwent alkaline texturing, single-sided polishing and RCA clean process. The BSG-SiO_x was deposited by atmospheric pressure chemical vapour deposition (5500 Series, Schmid, Germany) on the polished side of the wafers (Figure 1(a)). And then, the n^+ FSF and p^+ emitter formed simultaneously in a conventional liquid phosphorus trichloride ($POCl_3$) diffusion tube, we called the process co-diffusion (Figure 1(b)). It should be noted that an *in-situ* thermal oxidation procedure to grow SiO_x was introduced after the $POCl_3$ co-diffusion process. In this case, the PSG-SiO_x on the front side and BSG-SiO_x on the back side play the role of the protection layer in the next processes. Afterwards, local areas were ablated by a green picosecond laser (λ = 515 nm, f = 600 kHz) (LM1C-P30, Han's Laser, China) (Figure 1(c)). After the tetramethylammonium hydroxide (TMAH) chemical etching and RCA cleaning, P ions were implanted with an acceleration voltage of 15 keV and a dose of 3.0×10^{15} cm^{-2} on the quasi-planar rear side (IonSolar™, Kingstonesemi, China) (Figure 1(d)). The PSG-SiO_x on the front side and BSG-SiO_x on the back side were removed in a wet chemical etching step after the P implantation. And then, an effective annealing and oxidation process is done to repair the implantation damage and passivate the implanted surface. Please note that the annealing temperature of P implanted n^+ BSF is lower than the temperature that would be needed to anneal a B implanted p^+ emitter (which usually needs temperatures >1000 °C) [22,23]. We had employed five different temperatures (870, 900, 930, 960 and 990 °C) during the 30 min activation annealing and oxidation, resulting in ~3.5–5.0 nm SiO_2 on the p^+ emitter and n^+ BSF, together with a sheet resistance of n^+ FSF of 115 Ω/□, p^+ emitter of 51 Ω/□ and n^+ BSF of 28 Ω/□. Different thicknesses SiN_x:H (front side-75 nm, back side-90 nm) films were then deposited by plasma enhanced chemical vapour deposition (PECVD) (SINA XS, Roth & Rau, Germany) on both sides of the wafers (Figure 1(e)). Finally, contacts were ensured by the screen printing (LTCC, Baccini, Italy) of grids using Ag/Al and Ag pastes on the p^+ emitter and n^+ BSF areas on the back sides, respectively, with a co-firing in an infra-red belt-furnace (CFD-9024, Dispatch, USA) (Figure 1(f)).

2.2. Characterization

The morphologies of the silicon wafers were investigated by field emission scanning electron microscopy (Ultra plus, Zeiss, Germany). The doping profiles were measured by electrochemical capacitance-voltage profiling (CVP21, WEP, Germany) and the sheet resistance R_{sh} of the wafers were obtained by four-point probes (280I Series, Four Dimensions Inc., USA). The thickness and refractive index

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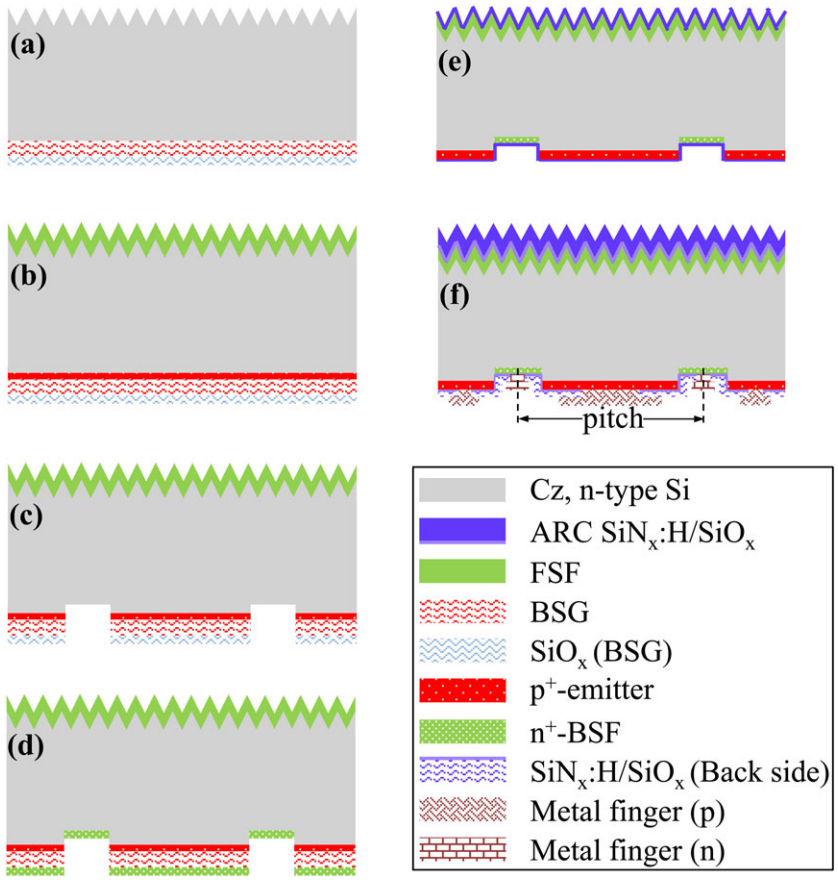

Figure 1. Schematic process sequences and structures for fabricating the back-junction back-contact (BJBC) silicon solar cells. (a) Surface wet chemical processes (front side textured and back side polished) and BSG/SiO_x deposited by atmospheric pressure chemical vapour deposition. (b) n^+ front side field (FSF) and p^+ emitter formed by co-diffusion. (c) Laser patterning and tetramethylammonium hydroxide (TMAH) etching in combination with RCA cleaning on back side of the wafers. (d) P ion implantation to the back side of the wafers. (e) Plasma enhanced chemical vapour deposition (PECVD)-SiN_x:H passivation stacks on three different doping areas after the annealing and oxidation process. (f) Back side metallization with Ag/Al on the p^+ emitter and Ag pastes on the n^+ back side field (BSF) by screen printing and co-firing technologies. [Colour figure can be viewed at wileyonlinelibrary.com]

of SiO_x and SiN_x:H thin films were determined by spectroscopic ellipsometry (SE400, Sentech, Germany). The saturation current density J_0 and implied open-circuit voltage (V_{oc}) were obtained by quasi-steady-state photoconductance method (WCT-120, Sinton Instruments, USA). The reflectance spectra as well as the internal quantum efficiency (*IQE*) were measured on the platform of quantum efficiency measurement (QEX10, PV Measurements, USA). The micrometre-level profiles of the surfaces of the silicon wafers were provided by 3D laser scanning confocal microscope (VK-9710, Keyence, Japan). The photoluminescence (PL) images were obtained by PL Tester (VS6840, Industrial Vision Technology (S) Pte Ltd., Singapore). The electrical parameters (V_{oc}, short-circuit current density J_{sc}, fill factor *FF* and energy conversion efficiency *Eff*) of the solar cells were analysed by current density–voltage (*J–V*) measurement under the illumination of AM 1.5 with I-V Tester (VS6821, Industrial Vision Technology (S) Pte Ltd., Singapore).

3. RESULTS AND DISCUSSION

3.1. Optical characterization of the front and back sides

Due to the absence of front metal electrodes, we can optimize the optical properties individually and make sure the BJBC solar cells harvest more light. We have employed the Wafer Ray Tracer [24] to calculate the total reflectance (R), substrate absorption (A), transmittance (T) and photogeneration current J_G for different surface morphologies. We emphasize that the thin film stacks' thicknesses of the front and back sides are from the experimental data (front side 75 nm-SiN_x:H/5 nm-SiO_2, back side 5 nm-SiO_2/90 nm-SiN_x:H), while the wavelength-dependent refractive indices are from McIntosh *et al.* [25]. Figure 2(a) shows that the total reflectance, substrate absorption and transmittance depend on the wavelength (300–1200 nm) for two different surface morphologies-front side textured and back side textured (FTBT) and front

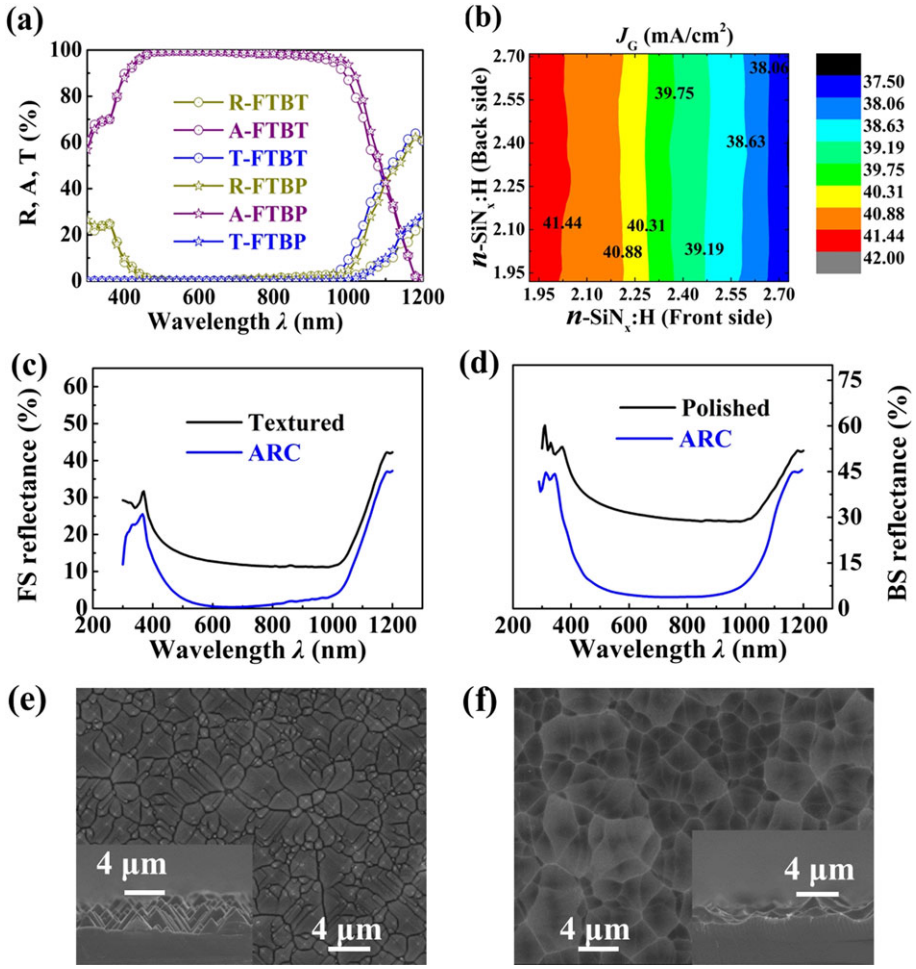

Figure 2. Optical and structural characterization of the front and back sides. (a) Simulated R (reflectance), A (substrate absorption) and T (transmittance) as a function of the wavelength λ for two different surface morphologies—front side textured and back side textured (FTBT) and front side textured and back side polished (FTBP) structures. (b) Photogeneration current J_G varies with the refractive index of the SiN_x:H antireflection coating (ARC). (c), (d) Experimental reflectance of the silicon wafer with the FTBP structural surfaces (front side—FS, back side—BS) before and after the PECVD-SiN_x:H ARC process. (e), (f) Micro-topographies of the front and back surfaces after the wet chemical processing. Shown in their insets is the side view of the two surfaces. [Colour figure can be viewed at wileyonlinelibrary.com]

side textured and back side polished (FTBP) structures. Obviously, the planar back side is more effective at reflecting the long wavelength light (>900 nm) back into the silicon wafer. In other words, we can expect more total reflectance and absorption as well as less transmittance when the back surface is planar structure (i.e., the FTBP case). Figure 2(b) displays the distribution of the photogeneration current J_G at different refractive indices of the SiN_x:H ARC with the FTBP surface, where the refractive indices of the front side play a dominant role and higher photocurrent J_G ($J_{G\text{-max}}$ = 41.71 mA/cm^2) can be realized at lower refractive indices ($n < 2.15$) of the stack films.

According to the above simulation results, we implement the silicon wafers with the FTBP structure using the wet chemical processing. After that, the front and back sides of the wafers are passivated by the thermal oxidation SiO_2 and PECVD-SiN_x:H stacks (front side 75 nm-SiN_x:H/5 nm-SiO_2, back side 5 nm-SiO_2/90 nm-SiN_x:H). We have achieved the lower refractive index (n = 2.05 at 632.8 nm) of the SiO_2/SiN_x:H stacks by means of adjusting the silane (SiH_4) and ammonia (NH_3) gas flow ratio. In order to characterize the effect of the light absorption on different surfaces (front side textured and back side polished), we present in Figure 2(c) and 2(d) the experimental reflectance of the silicon wafer with the front textured and back polished surfaces before and after the PECVD-SiN_x:H ARC process, respectively. We can find that the textured front surface and polished back surface exhibit low solar averaged reflectance of 2.5% in the wavelength range 450–1000 nm and 5.0% in the range 500–1000 nm, respectively. Figure 2(e) and 2(f) display an alkaline solution textured front surface with non-uniform pyramids size around 1–3 μm and acid solution

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polished back surface with irregular pits of depth less than 2 μm, respectively. In these conditions (different front and back surface morphologies, passivated film stacks with moderate thickness and low refractive index), we have the potential to receive more incident rays, higher photogeneration current J_G and conversion efficiency of the solar cells based on the optical optimization [10].

3.2. Doping areas optimization of the front and back sides

To evaluate the performance of the different highly doped areas (n^+ FSF, p^+ emitter and n^+ BSF), the saturation current densities J_0 were measured after using different drive-in times (1.5, 2.0 and 2.5 h) during co-diffusion (~930 °C) as well as during annealing oxidation (~930 °C) after P ion implantation. We have employed symmetrical textured structure (FSF) with 5-nm SiO_2/75-nm SiN_x:H stacks and polished structures (emitter, BSF) with 5-nm SiO_2/90-nm SiN_x:H stacks to test the recombination parameters J_0s of the n-type Cz silicon wafers (Figure 3(a)). A quasi-steady-state photoconductance lifetime tester was used to monitor the J_0 of the symmetrical wafer structures (Figure 3(b)) and the implied V_{oc} of the precursors (the silicon wafers before the metallization process) (Figure 3(c)). The saturation current density J_0s can be extracted by Kane and Swanson [26] method with a corresponding intrinsic carrier concentration n_i of 8.6×10^9 cm^{-3} and a high-level injection density Δn of 1.0×10^{16} cm^{-3}.

Considering that the different drive-in times (1.5, 2.0 and 2.5 h) have little effect on the J_0 of the emitter (E), we have taken the group E as the reference baseline to the groups FSF (F-1, F-2, F-3) and BSF (B-1, B-2, B-3) in Figure 3(b). Apparently, we can observe the optimum drive-in time of 2.0 h, where the average J_0 reaches 7, 16 and 21 fA/cm^2 for the FSF, emitter and BSF structures, respectively. In addition to the drive-in time, annealing temperature is also one of the important parameters to the properties of the BJBC silicon solar cells. Therefore, after the co-diffusion, laser patterning, TMAH etching in combination with RCA cleaning and P ion implantation to form the n^+ FSF, p^+ emitter and n^+ BSF in the same wafer, we have carried out five different annealing temperatures (870, 900, 930, 960 and 990 °C) for 30 min to activate and oxidize these doping areas. Afterwards, different thicknesses SiN_x:H (front side-75 nm, back side-90 nm) films were deposited by PECVD on both sides of the wafers. Figure 3(c) shows the implied V_{oc} of the BJBC silicon solar cell precursors for different annealing temperatures, measured after a sintering step similar to that used for contact formation (~905 °C, 30 s). Obviously,

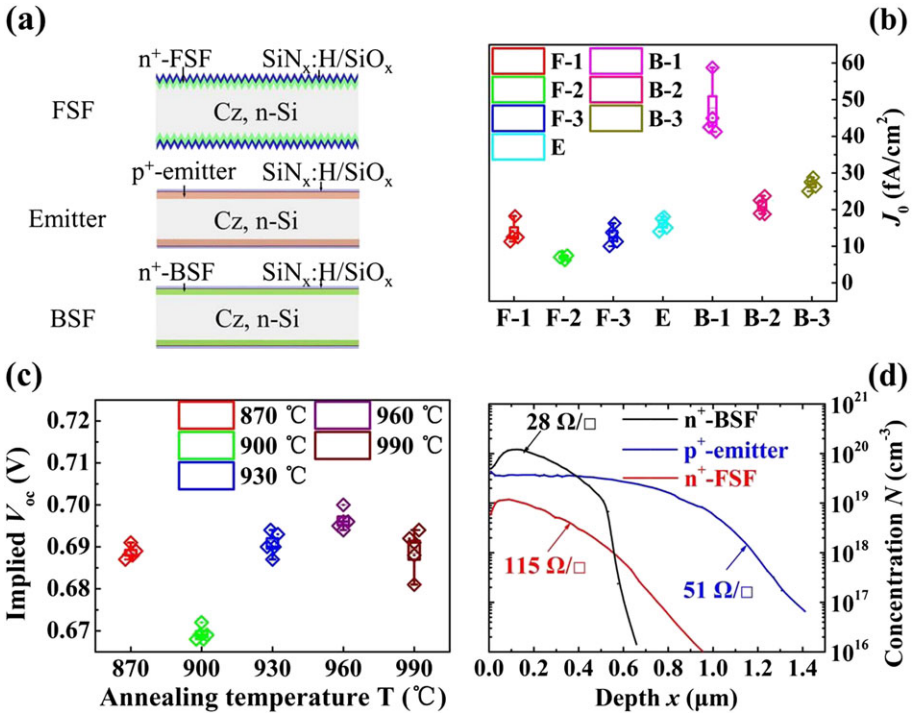

Figure 3. Doping areas optimization of the front and back sides. (a) Schematic diagram of the symmetrical structures (FSF, emitter, BSF) to test and extract the dark saturation current density J_0 of the n-type Cz silicon wafers. (b) J_0 of different doping areas (FSF, emitter, BSF) after three drive-in times (1.5, 2.0 and 2.5 h), with F-1, F-2 and F-3 for the FSF-1.5 h, FSF-2.0 h and FSF-2.5 h, as well as the same for the BSF case. (c) Implied V_{oc} of the precursors after different annealing temperatures (870, 900, 930, 960 and 990 °C). (d) Electrochemical capacitance-voltage dopant profiles of the n^+ BSF, p^+ emitter and n^+ FSF after the annealing temperature of 960 °C (30 min). [Colour figure can be viewed at wileyonlinelibrary.com]

the maximum implied V_{oc} of 0.700 V has been obtained on the BJBC solar cell precursors at the annealing temperature of 960 °C, where both the average implied V_{oc} of 0.695 V and the convergence of the implied V_{oc} are better than the other groups.

Figure 3(d) presents the electrochemical capacitance-voltage dopant profiles of the n^+ BSF, p^+ emitter and n^+ FSF after the annealing temperature of 960 °C (30 min). The P ion implantation yields a shallow n^+ BSF of 0.65 μm with the sheet resistance R_{sh} = 28 Ω/□ and a surface concentration of ~4.23×10^{19} cm^{-3}. The co-diffusion p^+ emitter (R_{sh} = 51 Ω/□) exhibits a surface concentration of ~4.35×10^{19} cm^{-3} with a junction depth up to 1.40 μm and n^+ FSF (R_{sh} = 115 Ω/□) displays a relative low surface concentration (~5.24×10^{18} cm^{-3}) and moderate junction depth (0.95 μm).

3.3. Laser patterning preparation for the formation of the n^+ back side field

In our study, we use a green picosecond laser (λ = 515 nm, f = 600 kHz) ablation rather than the photolithography to realize the interdigitated pattern on the back side of the silicon wafers. The introduction of the ultra-short pulse laser technology reduces the process sequence and saves the manufacturing costs. In view of the unique structural characteristics of the BJBC solar cells, the photogenerated minority carriers have to be transported vertically and laterally (especially above the BSF areas) to the collecting emitters on the back sides of the solar cells [27]. The collecting probability of the carriers generated above the BSF areas will decrease due to the wide BSF regions. We regard this effect as the electrical shading [28,29]. In order to reduce the transport loss, the design for narrow BSF and large emitter fraction on the back side of the silicon wafers is of greatest importance [30,31].

The laser with high flexibility and spatial resolution (the accuracy of less than 25 μm) locally ablates the BSG/SiO_x layer on the back side and define the BSF regions (Figure 4(a)). The width of the BSF region in a unit cell (2.02 × 2.02 cm^2) is about 500 μm with a constant metal contact pitch of 1.55 mm, i.e., a wide emitter of ~1050 μm. This pitch size and emitter coverage ratio on the back side represents the best trade-off between series resistance losses due to the lateral distances [32] and the resolution and positioning accuracy of the subsequent screen-printing metallization. There are 25 pieces of unit cells in every silicon wafer after the laser

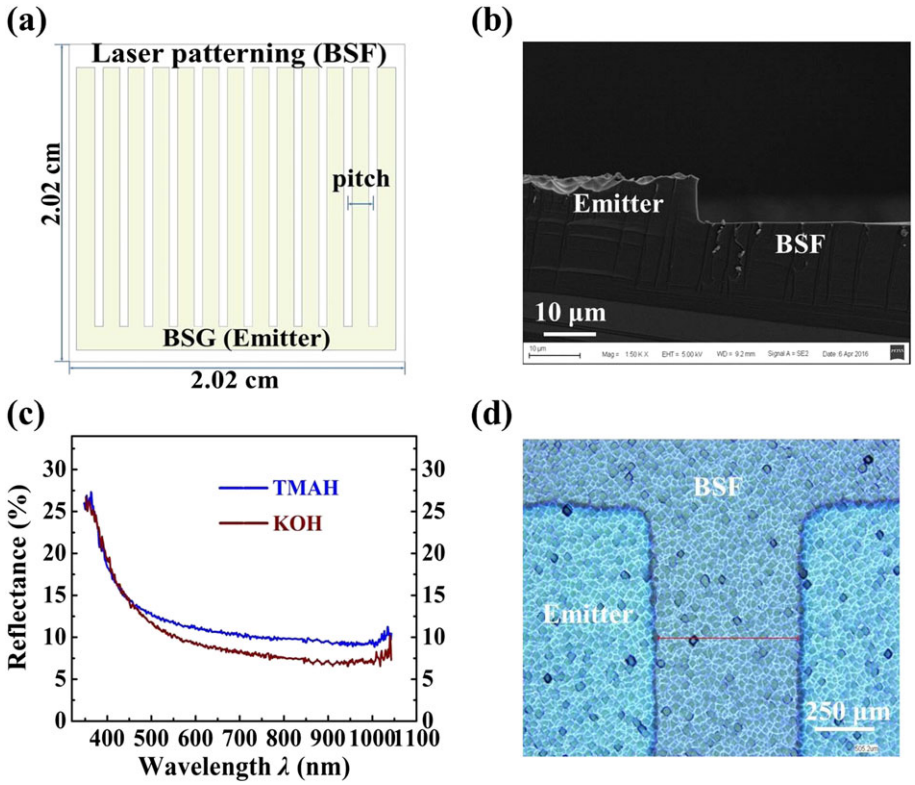

Figure 4. Laser patterning preparation for the formation of the n^+ BSF area. (a) An interdigitated structural pattern (BSF and emitter area) formed in a unit cell with the edge length of 2.02 cm by a picosecond laser ablation. (b) Scanning electron microscopy side view of the back side of the silicon wafer after the TMAH etching processes. (c) Reflectance of the laser damage surface from two different alkali (TMAH and potassium hydroxide (KOH)) solutions under the same conditions (25% wt., 65 °C and 35 min). (d) Difference between the BSF and emitter area on the back side of the silicon wafers after the TMAH etching shown by 3D laser scanning confocal microscope. [Colour figure can be viewed at wileyonlinelibrary.com]

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ablation patterning. We remove the laser-induced damage areas during the structure selective etching in a 25% wt. TMAH based solution at 65 °C for 35 min. The remaining BSG/SiO_x layer protects the p^+ emitter junction and acts as an etching barrier. In this way, an interdigitated structure with a height difference about 8 μm between the emitter and BSF (Figure 4(b)) is realized on back side of the silicon wafers. The surface of the emitter is still quasi-planar, whereas the BSF region is much smoother after the TMAH etching. The vertical separation of the emitter and BSF region prevents tunnelling recombination currents in gap-free BJBC solar cells and maximizes the short-circuit current density [33]. Furthermore, this gap-free structure eliminates the mask process and therefore simplifies the fabrication sequence. In this case, we have also compared the two different kinds of alkali (TMAH and potassium hydroxide (KOH)) solutions etching the laser damage region under the same conditions (25% wt., 65 °C and 35 min) and obtained that the reflectance of the laser damage surface is higher in TMAH than that in KOH solution (Figure 4(c)). Figure 4(d) shows the difference between the BSF and emitter on the back side of the silicon wafers after the TMAH etching by 3D laser scanning confocal microscope. Clearly, the width of the BSF region is observed to be about 505.2 μm, as designed.

3.4. Optimization of the screen-printing metallization

Because the metal fingers and bus bars are located on the back side of the BJBC silicon solar cells, they can be much wider than for conventional solar cells, as they will not cause optical shading. Wider fingers in BJBC solar cells can reduce resistive losses [7] and also increase the amount of long-wavelength light that is reflected back into the Si wafer [10]. In the present work, different metallization pastes (Ag and Ag/Al) form the corresponding electrical contacts for the n^+ BSF and p^+ emitter on the back side of the solar cells by the screen printing technology, and the metallization coverage ratio on the back side of the BJBC solar cells is as high as about 20%. Due to the resolution and positioning accuracy of the screen-printing metallization with the different coverage of the BSF and emitter areas, Ag paste is printed first on the n^+ BSF area, and then Ag/Al paste is printed on the p^+ emitter region. Afterwards, the Ag and Ag/Al pastes fire through the passivation stack layers SiO_2/SiN_x:H to form the good Ohmic contact with the silicon substrates in a co-firing step (the peak firing temperature of 905 °C, 30 s). Figure 5(a) clearly shows the different widths of fingers (~80 μm and ~280 μm) distributed in the BSF and emitter areas, respectively.

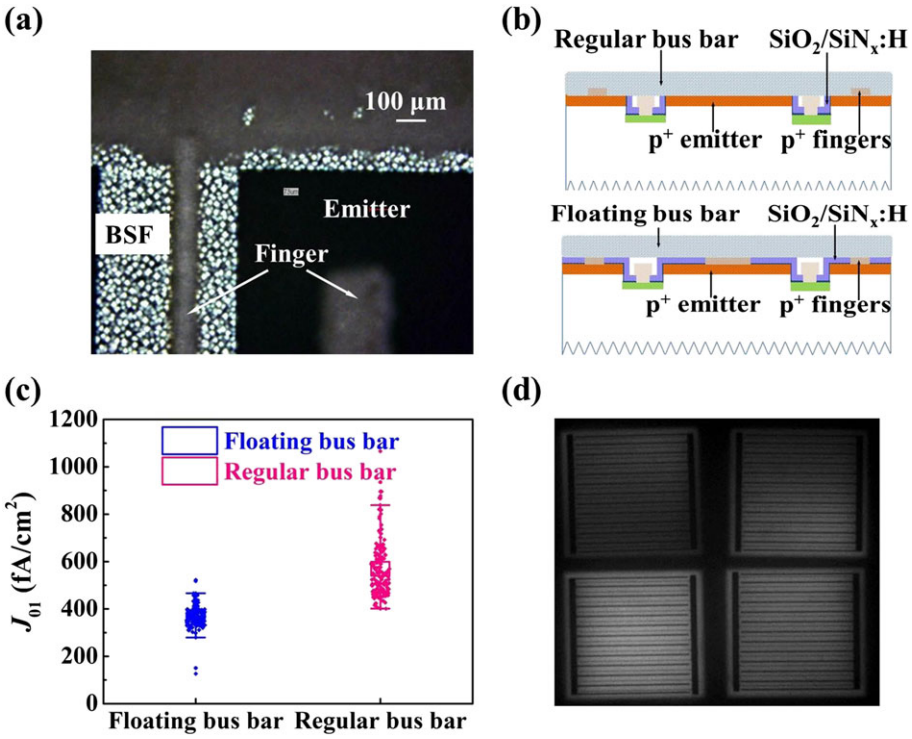

Figure 5. Optimization of the screen-printing metallization. (a) Different widths of fingers (~80 and ~280 μm) distributed in the BSF and emitter areas, respectively. (b) Schematic cross sections of the two kinds of different bus bar configurations (regular and floating bus bars) for minimizing the emitter contacts losses. (c) Compared sum of the saturation current density J_{01} from the emitter J_{0e} and the base J_{0b} between the two different metal bus bars. (d) Photoluminescence (PL) images of four pieces of the BJBC silicon solar cells taken at 1-sun injection level. [Colour figure can be viewed at wileyonlinelibrary.com]

The fire-through Ag/Al paste could damage the emitter junction area and lower the V_{oc} of the solar cells [34]. In order to decrease the emitter contacts losses, we design a new type of floating bus bar configuration and compare with the regular bus bar. The difference between the regular bus bar configuration and the floating bus bar design lies in whether the bus bar of the emitter area fires through the SiO_2/SiN_x:H stacks or not. This novel floating bus bar will not fire through the passivated layers (Figure 5(b)). As we know, the J_{01} can often be represented as the sum of the saturation current density of the emitter J_{0e} and that of the base J_{0b} [35,36]. We can extract J_{01} from Suns-V_{oc} [37] measurements to evaluate the quality of the emitter junction with these two different metal bus bars. Figure 5(c) demonstrates that the average J_{01} reduces to less than 400 fA/cm^2 in the floating bus bar design from the regular bus bar case over 500 fA/cm^2. We can therefore conclude that the solar cells with floating bus bars have less emitter-metal recombination losses.

Figure 5(d) displays the PL images of four pieces of the BJBC silicon solar cells taken at 1-sun injection level showing the relative luminescence intensities of each area of the solar cells. Notably, the luminescence intensities are relatively bright in the emitter and BSF areas indicating the high doping uniformity and good passivation effect. Whereas, the areas with metal contacts exhibit very low luminescence intensities (almost dark), suggesting very high metallization recombination losses there [38].

3.5. Performances of the back-junction back-contact solar cells

Because both the p- and n-bus bars of the BJBC silicon solar cells are placed on the back sides, the conventional measurement method (including the test tool) is infeasible. It is necessary to design a specialized measurement device to evaluate the electrical performances of the BJBC solar cells. Figure 6(a) shows the measurement stage for our BJBC solar cells in house. During the measurement, we have used the steady-state solar simulator (3A Class, Yamashita, Japan) under the AM 1.5 spectrum with illumination intensity of 1000 W/m^2 and kept the constant temperature of 25 °C. The real sizes of the finished solar cells (Figure 6(b)) are larger than the illuminated area (4.04 cm^2). The opening edge of the device is used to fix and balance the solar cell. Figure 6(c) exhibits the performances of the best produced cell (4.04 cm^2 with the efficiency of 22.20%, V_{oc} of 0.660 V, J_{sc} of 42.82 mA/cm^2 and *FF* of 78.56%) independently confirmed by SERIS. Figure 6(d) presents the *IQE*, external quantum efficiency (*EQE*) and the total reflectance for the finished BJBC silicon solar cell (2.02 × 2.02 cm^2). In the scope of the short wavelength (300–500 nm), the good *IQE* value (>85%) attributes to the high quality pyramids textured and passivated ARC front surfaces. The high *IQE* (over 98%) in the scope of the medium-long wavelength (500–900 nm) demonstrates the good carrier collection

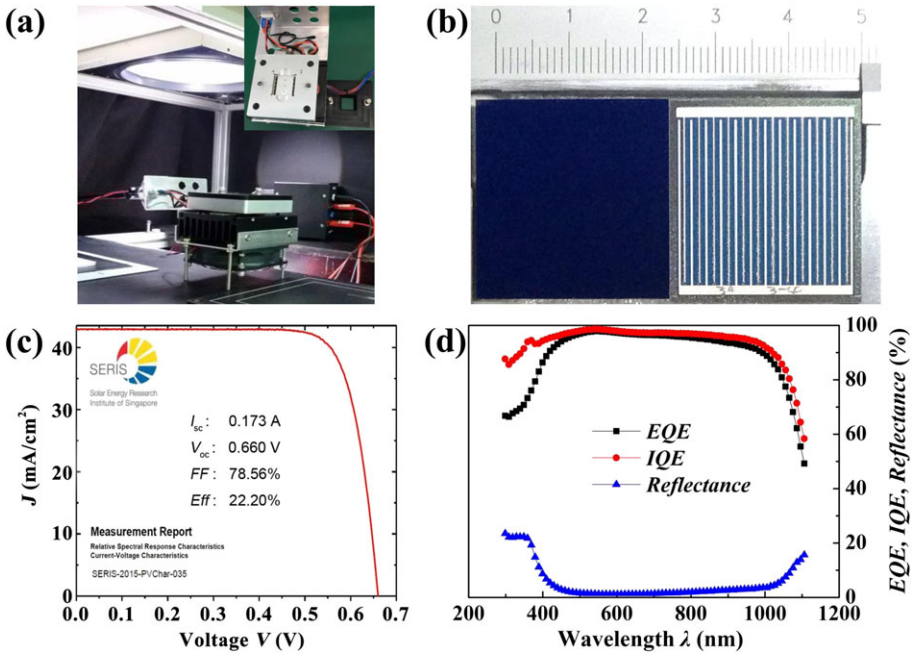

Figure 6. Performances of the BJBC silicon solar cells. (a) Measurement stage for BJBC solar cells with control-temperature equipment (constant temperature of 25 °C) and steady-state solar simulator (AM 1.5 spectrum with illumination intensity of 1000 W/m^2). (b) Physical photographs of the front (left) and back (right) side of the BJBC silicon solar cells. (c) *J–V* curve and characteristics of the best BJBC silicon solar cell (4.04 cm^2 with the efficiency of 22.20%), independently confirmed by Solar Energy Research Institute of Singapore (SERIS). (d) Internal quantum efficiency (*IQE*), external quantum efficiency (*EQE*) and total reflectance for the best BJBC silicon solar cell. [Colour figure can be viewed at wileyonlinelibrary.com]

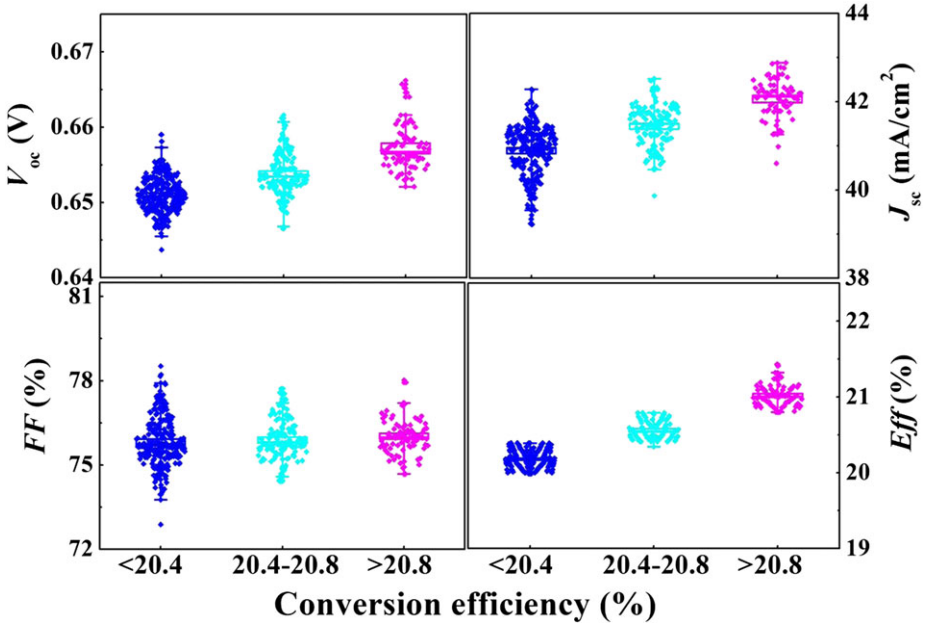

Figure 7. Electrical parameters (V_{oc}, J_{sc}, *FF* and *Eff*) statistical distribution for the 445 pieces of the BJBC silicon solar cells with size of 6 × 6 cm^2 under the three different grades of the conversion efficiency. [Colour figure can be viewed at wileyonlinelibrary.com]

throughout the cells, including the electrical shading areas [33]. We note that we can obtain the J_{sc} of 41.8 mA/cm^2 by means of integrating and folding the *EQE* with the AM1.5 spectrum, in good agreement with the maximum photogenerated current of 41.71 mA/cm^2 from the ray tracing simulations in Figure 2(b). This indicates that the value of 42.82 mA/cm^2 measured by SERIS is an overassessment of J_{sc}, also resulting in a slight overassessment of the efficiency (a J_{sc} of 41.8 mA/cm^2, a V_{oc} of 0.660 V and a fill factor of 78.56% result in an efficiency of 21.7%).

In order to verify the feasibility of the simplified industrial processes (co-diffusion, P ion implantation and annealing oxidation, laser patterning as well as screen printing and co-firing technologies), we have enlarged the sizes of the solar cells with the same manufacturing process flow and fabricated 445 pieces of the BJBC silicon solar cells (size 6 × 6 cm^2 with four bus bars). The average conversion efficiency Eff_{ave} of the 445 pieces BJBC silicon solar cells reaches over 20.4% (Eff_{min} = 19.99%, Eff_{ave} = 20.42% and Eff_{max} = 21.43%). We have divided the IBC solar cells into three different groups (<20.4%, 20.4–20.8% and >20.8%) according to the three different grades of the conversion efficiency of the finished BJBC solar cells. Figure 7 illustrates the electrical parameters (V_{oc}, J_{sc}, *FF* and *Eff*) distribution according to the three different grades of the conversion efficiency of the finished BJBC solar cells. The average V_{oc} reaches over 0.655 V, and the average J_{sc} exceeds 41.0 mA/cm^2. However, looking at Figure 7, almost half of the solar cells in the group >20.8% feature a J_{sc} above 42.0 mA/cm^2. As discussed above, the optical simulations suggest that the maximum J_{sc} should be around 41.8 mA/cm^2. This suggests that our in-house *J*–*V* measurements are overestimating J_{sc} by 0.5 to 1 mA/cm^2. The best 36 cm^2 BJBC solar cell has the characteristics of maximum *Eff* of 21.43%, V_{oc} of 0.6657 V, J_{sc} of 41.26 mA/cm^2 and *FF* of 78.02%. However, it should be noted that the *FF* distribution of all the BJBC silicon solar cells is in the range from 74.95 to 78.52%, and most of the *FF*s are under 76.50%. The low fill factor may be attributed to series resistance, shunt resistance and additional recombination currents (often described by J_{02} in the 2-diode-model) [39], and for the further improvement of the cell fill factors and conversion efficiency, it is necessary to optimize the screen printing (e.g., the resolution and positioning accuracy as well as double printing) and co-firing technologies to match with the unique structures of the back side of the BJBC silicon solar cells.

4. CONCLUSIONS

In summary, the conventional industrial processes have been employed to fabricate high performance BJBC silicon solar cells. We have successfully achieved the high efficiency of ~22% BJBC silicon solar cells with the size of 4.04 cm^2 using co-diffusion, P ion implantation and annealing oxidation, laser patterning as well as screen printing and co-firing technologies. In view of the characteristic configuration of the BJBC silicon solar cells (have no metal contacts on the front side), we have realized the good optical FTBP surface structures (low solar averaged reflectance of 2.5%) by means of software simulation and wet chemical processing. At the same time, we have obtained the average implied V_{oc} of 0.695 V of the BJBC silicon solar cell precursors by comparing the different drive-in times (1.5, 2.0 and 2.5 h) and annealing

temperatures (870, 900, 930, 960 and 990 °C) for 30 min. Furthermore, the high flexibility and spatial resolution ultra-short pulse laser patterning and screen-printing technologies provided a powerful support for realizing the back side metallization of the BJBC silicon solar cells. Finally, we have enlarged the size of the solar cells to 6 × 6 cm^2 with the same manufacturing process flow and achieved the maximum *Eff* over 21%. The present simplified cell structure has great advantages in the low-cost BJBC silicon solar cell industrialization and could be compatible with the existing production lines and processes.

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