

Electrical characterization of P3 isolation lines patterned with a UV laser incident from the film side on thin-film silicon solar cells

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ABSTRACT

We investigate the properties of P3 isolation lines in *a*-Si : H/*μ*c-Si : H solar modules, prepared with a nano-second pulsed UV laser incident from the film side of the solar module. For the electrical characterization of the P3 lines we developed a method which allows us to distinguish between leakage currents directly across the P3 line, leakage currents along the laser line side walls and to monitor changes in conductivity of the TCO underneath the line. We applied the developed characterization method to a series of P3 lines where we systematically varied the used laser parameters. In addition we analyzed selected P3 lines using Scanning Electron Microscopy. From the systematic variation we find that a high leakage current directly across the P3 lines is observed when the back contact is not fully removed. The best P3 lines have the back contact fully removed but an incomplete removal of the silicon in the line. When the silicon layer stack is fully removed in the P3 line we observe an increase in leakage current along the side walls of the laser lines. The best P3 laser line we obtained exhibits a very low leakage current density of only $1.5 \mu\text{A cm}^{-1}$ at 1 V.

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1. Introduction

One of the advantages of thin-film solar cells is the possibility to monolithically interconnect the module during the deposition process. To this end, deposition processes and scribing processes are applied alternately. In the commonly used laser scribing methods for thin film silicon solar modules the laser beam is incident through the (transparent) superstrate to remove the film. However, there are emerging flexible thin-film technologies where the solar cells are deposited on substrates such as plastics and metal foils [1–4]. For modules with opaque substrates the active layer and back contact layer cannot be removed with a laser beam incident through the substrate. Also for some transparent substrates a substrate incidence may be undesirable (e.g. some plastics or textured glass). In these cases a laser beam incident directly from the film side is required. The laser scribing of flexible thin-film solar modules faces several challenges like difficulties of producing abrupt edges of scribing grooves [5,6] and plume shielding [7]. Furthermore, on conductive substrates a monolithic interconnection requires the deposition of an insulating layer before producing the solar cell. All these issues make the film-side scribing more difficult to realize. These and other issues are discussed in detail in Refs. [4,8–10].

In this work we will discuss P3 laser scribing of thin-film silicon modules from the film side. A schematic drawing of the standard series connection in a thin-film silicon solar module in superstrate configuration is shown in Fig. 1. In the figure three laser lines are indicated, P1, P2 and P3, where the number refers to the processing order (i.e. P1 line is the first laser scribing process, P2 the second, etc.). The P1 line isolates the TCO electrodes of two neighboring cells. Similarly, the P3 lines isolate the back electrode of two neighboring cells. The P2 line is located between the two isolation lines and serves to make a contact between the front and back electrode. The P1 line is scribed before the deposition of the active layers. After the subsequent active layer deposition the P2 line is scribed. After the P2 step the back contact is deposited, followed by the P3 scribing step. In previous work we discussed the P1 and P2 scribing processes from the film side [9,11].

In this work we will focus on the last scribing step. Commonly, a green laser with wavelength of $\lambda = 532 \text{ nm}$ is used for P3 lines from the glass side. By scribing through the glass, the laser energy is absorbed in the silicon, starting from the interface between the silicon and the transparent conductive oxide (TCO). The silicon evaporates at the interface which causes an explosion which results in a clean removal of the silicon and the back contact. The laser energy required is much less than that is needed to thermally evaporate all the layers [12–14].

In this paper we use an optically pumped Nd:YVO₄ laser at the third harmonic with a wavelength of $\lambda = 355 \text{ nm}$ to pattern

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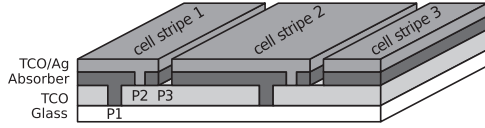


Fig. 1. Schematic drawing of series interconnection of thin-film silicon solar module.

P3 line from the film side. The advantage of using a shorter wavelength (UV) laser is the higher absorption coefficient in silicon and thus a shorter penetration depth. The UV laser is commercially available and has a pulse duration in the range of 10–20 ns.

We developed a method for the analysis of the quality of P3 lines. Using this analysis we characterize the P3 lines in terms of the separation of the back electrode, the introduction of shunts at the laser lines and the possible damage to the front electrode under the line. We systematically varied scribing parameters for P3 lines. The properties of the P3 lines were then electrically analyzed with the developed method. Furthermore, selected samples were analyzed using Scanning Electron Microscopy (SEM).

The paper is organized as follows. In Section 2 we present our experimental setup. The method we developed for the analysis of P3 lines is introduced in Section 3. In Sections 4 and 5 we present and discuss our results.

2. Experimental

2.1. Experimental setup

For the experimental P3 lines from the film-side we used a diode-pumped Q-switched Nd:YVO₄ laser source from Rofin-Sinar Technologies Inc. with a wavelength of $\lambda = 355$. The laser source was working in TEM₀₀ mode. The full width at half maximum pulse duration was $\tau_{pulse} = 10\text{--}20$ ns. The laser power was adjusted with an external attenuator. In this work the laser pulse repetition frequency was $f = 15$ kHz. A split-axis system allows positioning on the substrate plane with a resolution of 1 μm . The scanning speed of the XY-axis is up to 1 m/s. A linear Z-axis makes it possible to adjust the beam focus plane to the film surface.

Apart from the experimental laser lines we also applied our standard P1, P2 and P3 laser processes from the glass side. For these processes our laser setup is equipped with several diode-pumped Q-switched Nd:YVO₄ laser sources from Rofin-Sinar Technologies Inc. For the P1 process we used a laser with wavelength 355 nm. For the standard P2 and P3 processes we use the frequency doubled laser with a wavelength of 532 nm. More information on the standard laser patterning process see Refs. [15,16].

2.2. Pulsed laser patterning

Each laser pulse leaves a crater with radius r on the substrate. A laser beam with pulse repetition frequency f scans along the substrate with speed v , which gives a distance of $d = v/f$ between two neighboring crater centers (see Fig. 2). The pulse overlap number is defined as

$$O = \frac{2rf}{v} \quad (1)$$

To pattern a continuous laser line, we need to adjust the scanning speed or pulse repetition frequency such that $O \geq 1$. The overlap number is the number of laser pulses the center of the laser line receives during the scribing of the line. In order to achieve high-speed laser patterning (high scanning speed or high pulse repetition frequency), a low overlap number is favorable.

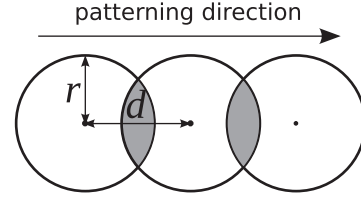
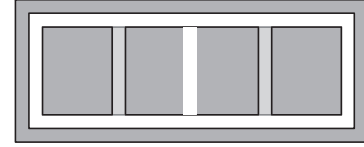


Fig. 2. Schematic illustration of pulsed laser patterning of laser lines.



However, depending on the layer thickness and the laser pulse energy, a certain minimum overlap ratio may be required to remove enough material from the line.

2.3. Substrate preparation

We patterned in-house developed thin-film $a\text{-Si} : \text{H} / \mu\text{c-Si} : \text{H}$ solar cells on commercially available rough Asahi U-type SnO₂ substrates. The Asahi U-type substrates have a thickness of around 850 nm with a root-mean-square (RMS) roughness of 40–50 nm. The $a\text{-Si} : \text{H} / \mu\text{c-Si} : \text{H}$ tandem cells were prepared without an intermediate reflector. The $a\text{-Si} : \text{H} / \mu\text{c-Si} : \text{H}$ layers were deposited with plasma enhanced chemical vapor deposition (PECVD) with a thickness of around 1300 nm (for more details, see Refs. [17,18]). The module back contact consists of sputtered ZnO (80 nm)/Ag(200 nm)/ZnO (80 nm) stacks.

Three series of experiments are applied to the samples where we varied the number of scribes for a line, S , the overlap number, O , and the laser pulse power, P . When we vary the number of scribes we set the pulse power to $P = 345$ mW (the total energy of a laser pulse is $E_p = 23 \mu\text{J}$) and the pulse overlap ratio to $O = 1$. The number of scribes for the line is varied between $S = 1$ and $S = 18$. In the overlap ratio series, we set the same pulse power ($P = 345$ mW) and we set $S = 1$. We adjusted the laser scanning speed to change the pulse overlap number. The overlap number is varied from $O = 1$ to $O = 9$. For the pulse power series we varied the power from $P = 43$ mW to $P = 860$ mW ($E_p = 2.9 \mu\text{J}$ to $E_p = 81.3 \mu\text{J}$). As the pulse power is not sufficient to remove the layer stack in a single pulse we set the overlap ratio to $O = 2$ and scribed twice ($S = 2$).

3. Electrical characterization of P3 isolation lines

To characterize test P3 isolation lines we developed the test structure depicted in Fig. 3. Shown are the top view in Fig. 3(a) and the cross-sectional view in Fig. 3(b). The test structure has four terminals, T1–4. We first deposit the absorber

layer on the glass/TCO substrate and two P2 lines are scribed using standard process. After the scribing of the P2 lines the ZnO/Ag/ZnO back contact layer stack is deposited. After this deposition we make the standard P3 lines from the glass side (c.f. Fig. 3). In a final step we isolate the test structure by scribing a line around the test structure removing the entire layer stack, this line is indicated with “P1+P3” in Fig. 3. For details on the standard process see reference [15]. The last scribe is the test P3 line scribed with a UV laser from the film side, which separates terminals T3 and T4. However, before we make the test scribe we measure several current/voltage characteristics so we can monitor the changes the scribing of the test line induces.

Before scribing the test P3 line we measure the current/voltage characteristics between terminals T1 and T2 (JV_{12}^b) terminals T1 and T3 (JV_{13}^b) and terminals T2 and T4 (JV_{24}^b). Characteristic JV_{12}^b reflects the conductivity of the TCO layer before the test scribe. Characteristics JV_{13}^b and JV_{24}^b both reflect the current/voltage characteristics of the solar cell before scribing the test line.

After scribing the test P3 line we measure again over terminals T1 and T2 (JV_{12}^a) terminals T1 and T3 (JV_{13}^a) and terminals T2 and T4 (JV_{24}^a). In addition we measure the separation over terminals T3 and T4 (JV_{34}^a). The resulting four current/voltage characteristics are modeled with the electrical circuit shown in Fig. 4. The model consists of four Voltage Controlled Current Sources (VCCSs), which are used to model the DC behavior of a two terminal device with an arbitrary current/voltage (JV) characteristic. The top component (JV_{Sep}) represents the connection between the back contacts of the two adjacent cells. Ideally, a P3 line separates the back contacts of two adjacent cells and thus the top component represents a parasitic leakage current that flows directly across the P3 line between the back electrodes. The bottom VCCS (JV_{TCO}) represents the connection between terminals T1 and T2 via the TCO after the test line. The left and right VCCS components (JV_{Dleft} and JV_{Dright}) represent the left solar cell and the right solar cell, respectively. These current/voltage characteristics include possible damage caused by the scribing of the test P3 line.

We developed an iterative algorithm to separate the electrical characteristics of each individual component in the circuit. First, we assume an initial JV characteristics for each component in the circuit. We then simulate the same four current/voltage characteristics we measured using a circuit simulator. The circuit simulator takes tabular voltage/current pairs as input data to form a piece wise linear current/voltage characteristic for each of the VCCS components in the circuit. We then iteratively adapt current/voltage characteristics of each component in the circuit to match the measured and simulated characteristics of the device.

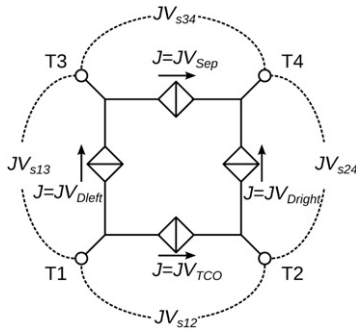


Fig. 4. Schematic of the circuit used to model the test device with the terminals T1–4 corresponding to the test structure in Fig. 3. Indicated are the four VCCS components, JV_{TCO} , JV_{Dleft} , JV_{Dright} , and JV_{Sep} . Using the circuit the JV curves are simulated over terminals T1 and T2, JV_{12}^a , T1 and T3, JV_{13}^a , T2 and T4, JV_{24}^a , and T3 and T4, JV_{34}^a .

We used the following iterative corrections:

$$JV_{TCO}^{i+1,j} = \frac{JV_{12}^j + nJV_{s12}^{i,j}}{(1+n)JV_{s12}^{i,j}} JV_{TCO}^{i,j} \quad (2)$$

$$JV_{Dleft}^{i+1,j} = \frac{JV_{13}^j + nJV_{s13}^{i,j}}{(1+n)JV_{s13}^{i,j}} JV_{Dleft}^{i,j} \quad (3)$$

$$JV_{Dright}^{i+1,j} = \frac{JV_{24}^j + nJV_{s24}^{i,j}}{(1+n)JV_{s24}^{i,j}} JV_{Dright}^{i,j} \quad (4)$$

$$JV_{Sep}^{i+1,j} = \frac{JV_{34}^j + nJV_{s34}^{i,j}}{(1+n)JV_{s34}^{i,j}} JV_{Sep}^{i,j} \quad (5)$$

where an s in a subscript indicates the current/voltage characteristics are simulated, the index i refers to the iteration and JV^j is the j -th current in the tabular set of current/voltage data. The parameter n is used to enhance convergence of the algorithm where the larger n is the smaller the iterative adaptations to each JV characteristic. Typically we initialize n with a large value (e.g. 10) to avoid oscillations in the iterative adaptations and gradually reduce the value of n to 0 as the number of iterations progress.

The algorithm is very simple to implement. We used the GNUcap circuit simulator for the circuit simulations [19]. The circuit simulator is called from a GNU Octave [20] script which implements the iterative algorithm. The method has the advantage that we directly use tabular data to describe the current/voltage characteristics of the components in the circuit, thereby making minimal assumptions about the nature of our devices. However, we did impose one restriction to the current/voltage characteristics of the components, namely that the current is monotonously increasing with applied voltage. This ensures that there is only one unique solution for the currents and voltages in the circuit and generally also improves the numerical stability of the circuit simulation. This restriction is implemented by sorting the current data in ascending order after each iterative refinement, without re-ordering the voltages.

We found in working with experimental data that our method initially converges monotonously, i.e. the discrepancy between measured and simulated current/voltage characteristics reduces steadily. However, after the initial convergence the error between simulation and experiment becomes rather erratic, varying seemingly random from iteration to iteration. However, in many cases the fit can still be improved upon at this stage by letting the algorithm iterate for a while and afterwards selecting the best fit from all previous iterations.

As a last step we compare the device before and after scribing the test P3 line. A change in conductivity of the TCO can be seen directly from a change in JV_{12} before and after the test line. The test P3 line may also induce damage to the solar cell in the line and its direct vicinity. We therefore compute the current that flows along one sidewall of the test line (the line has two sidewalls, left and right)

$$JV_{sw} = \frac{JV_{Dleft} + JV_{Dright} - JV_D^b}{2} \quad (6)$$

where JV_D^b is the current/voltage characteristic of the solar cell before the test line which is computed by averaging the currents in JV_{13}^b and JV_{24}^b . Note that we compare the solar cell before the test scribe with the sum of the currents through the two solar cells after the test scribe (i.e., T3+T4) where we neglect the loss of surface area of the test P3 line as its surface is small compared to the area of T3+T4 (the area of T3+T4 is $5 \times 10^{-1} \text{ cm}^2$ compared to the area of the test P3 line which is $2.5 \times 10^{-3} \text{ cm}^2$). Note that the total leakage current induced by a P3 line consists of $J_{sh} = J_{sw} + J_{Sep}$.

4. Results

In Fig. 5(a) we show a typical measurement of the four current/voltage characteristics after scribing a test P3 line. The typical measurement comes from the overlap number series and corresponds to $O=5$. The characteristic JV_{12}^a has an ohmic character and exhibits the highest conductivity of the measured JV characteristics. The JV characteristics JV_{13}^a and JV_{24}^a both show properties of a diode. For voltages above 1.1 V, JV_{13}^a and JV_{24}^a are approximately the same, whereas at lower bias voltages both exhibit the characteristics of a parallel resistance. The parallel resistance in JV_{13}^a is smaller than the parallel resistance in JV_{24}^a . The separation measured over terminals T3 and T4 (JV_{34}^a) is approximately ohmic and below a voltage of 1.1 V this characteristic coincides with JV_{24}^a .

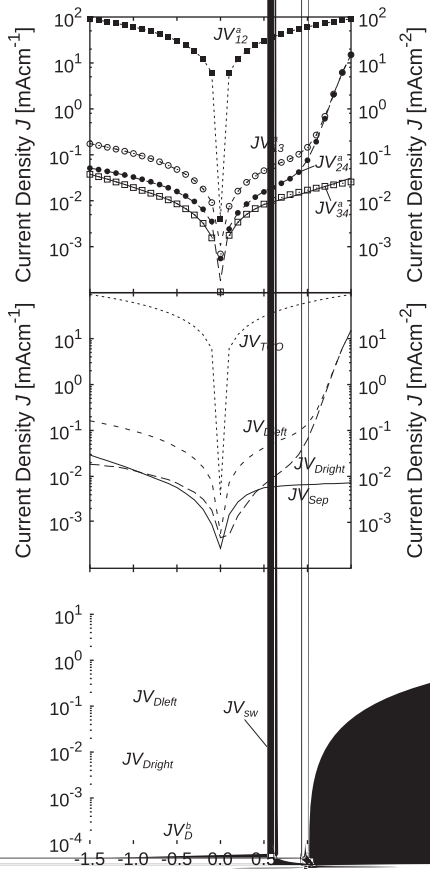
The dashed lines in Fig. 5(a) are the simulated current/voltage characteristics with the procedure outlined in Section 3. A consistent fit is obtained with a Root-Mean-Square (RMS) relative error of about 7%. In Fig. 5(b) we show the extracted current/voltage characteristics of the components in the equivalent circuit of Fig. 4. Characteristic JV_{TCO} is more or less the same as JV_{12}^a . Furthermore, the left side of solar cell JV_{Dleft} is approximately the same as JV_{13}^a , indicating that JV_{13}^a is dominated by the left side of the solar cell. However, the right side of the solar cell, JV_{Dright} does not coincide with JV_{24}^a . The separation, JV_{Sep} , is approximately

identical to JV_{34}^a . From this it follows that the current in the characteristic JV_{24}^a below 1.1 V flows predominantly via the components JV_{Sep} , JV_{Dleft} and JV_{TCO} , rather than directly through JV_{Dright} .

We compare the properties of the test structure before and after scribing the test line. We find no difference between JV_{12}^a and JV_{12}^b (not shown). We therefore conclude the TCO under the test line is not damaged to the extent it is relevant for the series connection. Fig. 5(c) shows the diode before the test line, JV_D^b , and the diode on the left and right side of the test line, JV_{Dleft} and JV_{Dright} , respectively. Using Eq. (6) we determine the sidewall current density. Note that the sidewall current is the average current flowing along the left and right sidewalls. We cannot distinguish between the left and right sidewall currents because we cannot distinguish between the left and right side of the diode before the scribing of the test line. However, in this case the diode before the test line exhibits lower currents for voltages below 0.8 V than both diodes on the left and right side of the test scribe. This indicates that the differences between the JV_{Dleft} and JV_{Dright} below 0.8 V stem from differences between the left and right side of the sidewall.

In Fig. 6(a) we show the current density along a sidewalls of the test P3 lines for the overlap number series. In the series we varied the overlap number from $O=1$ to $O=9$. A clear distinction can be made between $O \leq 4$ and $O > 4$. For an overlap number larger than 4 the sidewall current is considerably larger than for an overlap number below 4 for voltages up to 1.2 V. Fig. 6(b) shows the separation characteristic. The separation current density decreases with the overlap number for $O \leq 4$. The difference in the separation current density is almost 4 orders of magnitude between $O=1$ and $O=4$. For an overlap number $O > 5$ the JV_{Sep} cannot be determined accurately because the current density in JV_{34}^a is then dominated by the current that flows via JV_{Dleft} , JV_{TCO} , and JV_{Dright} . For this reason we omitted JV_{Sep} from Fig. 6(b) for $O > 5$.

The other two series show similar trend to the overlap number series. With increasing pulse power or number of scribes the



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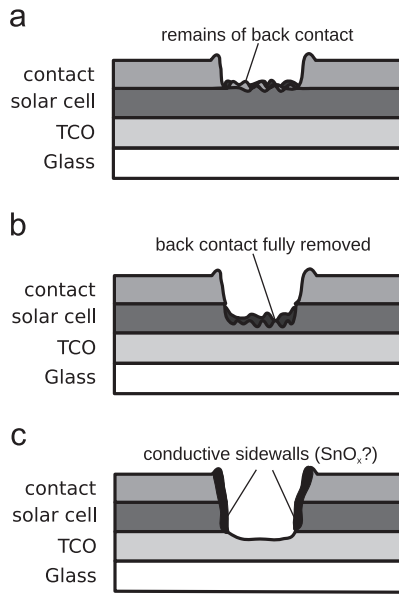


Fig. 9. Schematic illustration of P3 laser lines. (a) P3 line for low power/overlap number/number of scribes. The line exhibits a low JV_{sep} resistance and a high JV_{sw} resistance. (b) P3 line for optimal power/overlap number/number of scribes. The line exhibits high JV_{sep} and JV_{sw} resistances. (c) P3 line for a power/overlap number/number of scribes beyond the optimum. The line exhibits a high JV_{sep} resistance and a low JV_{sw} resistance.

there is a long time between successive scribes leaving ample time for the line to cool down. The higher temperatures for a high overlap number lead to more damage to the sidewalls and/or TCO splashed out of the line.

6. Conclusions

In this paper we investigated laser scribing of P3 isolation lines for $a\text{-Si:H}/\mu\text{-Si:H}$ solar modules from the film side with a nano-second pulsed UV laser. We developed a method to characterize the electrical properties of the experimental P3 lines. With this method we can distinguish between leakage currents directly across the P3 line, leakage currents along the laser line sidewalls and monitor changes in conductivity of the TCO underneath the line. We systematically varied scribing parameters for P3 isolation lines with a UV laser incident from the film-side. The properties of the resulting P3 lines were electrically analyzed with the developed method. In addition we examined selected P3 lines using Scanning Electron Microscopy images. We find that the best P3 lines have the back contact fully removed but an incomplete removal of the silicon in the line. If the silicon in the line is fully removed we observe an increase in the leakage current which we could ascribe to currents flowing along the sidewalls of the laser lines. For an incomplete removal of the back contact we observe a leakage current directly across the P3 line.

The best P3 laser line we obtained with the systematic variation of laser parameters exhibits a very low leakage current density of only $1.5 \mu\text{A cm}^{-1}$ at 1 V (current per unit laser line length).

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