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Revealing the effect of phosphorus diffusion gettering on industrial silicon heterojunction solar cell

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ABSTRACT

Here we have conducted a comprehensive experimental and theoretical investigation into the impact of the phosphorus diffusion gettering (PDG) process on n-type industrial silicon heterojunction (SHJ) solar cells. Our findings indicate that phosphorus penetrates deeply into the silicon substrate as circular channels. While PDG effectively eliminates Fe from silicon wafers, it also introduces impurities like O, P, and Cu, which are not entirely eradicated during subsequent cleaning and texturing processes. Optimizing the gas flow to 1000 sccm achieved a balance between carrier lifetime and saturated dark current density in SHJ solar cells, resulting in a 0.21 % increase in average efficiency to 25.14 %. Simulated analyses revealed that variations in energy loss due to different gas flows were primarily attributed to bulk recombination and series resistance. Our work provides valuable insights for the application and improvement of the PDG process in industrial SHJ solar cells.

1. Introduction

As a key technology for carbon neutrality, crystalline silicon solar cells consistently account for more than 90 % of the photovoltaic market [1]. Photovoltaic power conversion efficiency (PCE) has made great progress over the past decades with a growth rate of 0.5%–0.6 % per year, which resulted in p-type wafers no longer meeting the requirements of technological advances [2,3]. Consequently, the replacement of n-type wafers for p-type wafers has been initiated in recent years, with n-type devices mainly containing two types: the tunnel oxide passivation contact (TOPCon) and silicon heterojunction (SHJ) solar cells [4–7]. With SHJ technology, the peak PCE records attained are 26.8 % [8] for bifacial contact and 27.3 % for integrated back contact [9]. Despite steady PCE growth, SHJ solar cells are becoming increasingly sensitive to defects and impurities in the silicon wafer as back-junction devices [10–12].

Considering industrial cost constraints, the purity of silicon for photovoltaics is inherently low, with additional impurities being introduced during the manufacturing process [11]. Metallic impurities are one of the main recombination losses in silicon substrates, leading to a decrease in the PCE of solar cells [13–15]. Phosphorus diffusion gettering (PDG) has been most widely used in silicon photovoltaic technology due to its high capture efficiency and metal mobility at high temperatures [16–19]. It has been demonstrated that PDG effectively enhances the efficiency for p-type crystalline silicon solar cells, especially for p-type multicrystalline silicon [20–24]. By substantially reducing metal impurity concentrations, especially the iron pollution, the PDG process greatly enhances the effective minority carrier lifetime [13,25,26]. Relatively speaking, there are few PDG reports on n-type silicon wafers. Macdonald et al. have studied the industrial n-type silicon ingot grown by the rechargeable Czochralski method, and have revealed its high carrier lifetime and excellent electronic quality close to the Auger limit [27]. The remarkable progress underscores the effectiveness of PDG in impurity removal and highlights the already high baseline quality of industrial silicon wafers [28]. Despite the higher cost, n-type monocrystalline silicon has gradually become a mainstream

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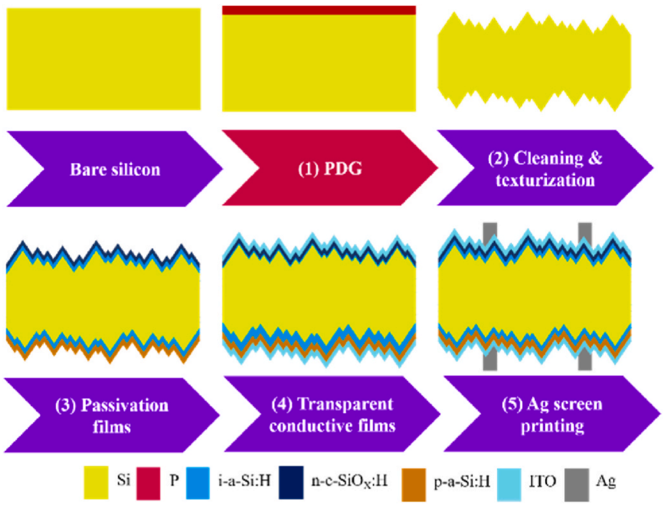

Fig. 1. (a) The industrial fabricated process for SHJ solar cell including front PDG treatment.

photovoltaic material in recent years, owing to its high electron mobility, long carrier lifetime, and reduced photodegradation [7,29,30].

In the case of TOPCon solar cells, there is no traditional n^+ emitter to perform gettering. Instead, n^+ poly-Si contacts are introduced to provide a gettering effect by capturing metallic impurities during the high-temperature annealing process [31]. This highlights the importance of tailored gettering strategies in modern high-efficiency silicon solar cells and provides a basis for exploring similar mechanisms in SHJ technologies.

Unlike the traditional solar cell [32,33], the maximum processing temperature of SHJ device is generally around 200 °C due to the poor temperature tolerance of hydrogenated amorphous silicon films and transparent conductive films [30,34]. As a result, the PDG process had to be scheduled for SHJ solar cell before the wet chemical process. In recent years, there have been only a few researchers, such as Zhengxin Liu team [35] and Rabin Basnet team [36], who have performed PDG in different quality wafers for n-type SHJ solar cell and achieved excellent efficiency improvement of 0.4–3.2 %. Nevertheless, the PCE of prepared devices is lower than 23 % after PDG treatment, weakening the significance of their findings as a guide for practical production, owing to the fact that the effect of PDG decreases as the PCE of solar cells increases. More importantly, the microscopic morphology of diffusion and the effective region for the gettering of PDG process in SHJ solar cells remains largely undisclosed.

In this work, we achieved an average PCE exceeding 25 % for industrial SHJ solar cells (>1800 samples per group) with a PCE improvement of 0.2 % using the preferred PDG process. Additionally, surface morphology observations revealed that P diffusion is not uniform across the whole plane. Using combined XRF and TOF-SIMS characterizations, we demonstrated elemental changes during the PDG process and detected impurity residues after texturing. Moreover, the gettering effect is mainly concentrated at the half-edge position of the substrate exposed through the PL mappings. We then systematically analysed and compared the optical and electrical properties of the silicon substrate as well as the SHJ solar cells at different gas flows. Free energy loss simulations also were performed using Quokka2 software to visualise the role of the PDG process.

2. Experiments and simulations

2.1. Device fabrication

Monocrystalline n-type Czochralski silicon wafers (182 mm × 91 mm × 120 μm) with resistivities ranging from 1.5 to 4.5 Ω cm were chosen to verify the effectiveness of PDG. Fig. 1 illustrates the preparation process on the front side of the SHJ solar cell. Initially, the PDG process was conducted in an ample O_2 environment at temperatures ranging from 780 to 890 °C. Both the loading and unloading temperature zones were maintained at 780 °C. After evacuating the chamber, the temperature was increased from 780 °C to 805 °C, where O_2 and N_2-carrying $POCl_3$ were introduced for phosphorus diffusion. The chamber pressure was controlled by another N_2. The flow ratio of O_2 and N_2-carrying phosphorus liquid source gas was 1:2. Another N_2 gas was introduced to regulate the pressure of the chamber at the same time. The exact flow rates of N_2-carrying gas were varied (0, 500, 1000, 2000 sccm) to evaluate their impact on the performance of SHJ solar cells. The temperature was then allowed to rise to 890 °C to advance deeper into P diffusion at a higher temperature. Then, the temperature was lowered to 780 °C to conduct gettering. The whole process lasted 60 min, after which the vacuum was removed and the sample was pushed outside the chamber to cool naturally.

Next, the surface damage of the silicon wafer, with or without PDG, was removed by immersing it in a mixture of KOH and H_2O_2. Following the removal of surface damage, the wafers were etched with KOH solutions to create micron-pyramids, and subsequently cleaned and dried. Afterwards, bifacial intrinsic (i) hydrogenated amorphous silicon (a-Si: H) films were separately prepared by the plasma enhanced chemical vapor deposition (PECVD), followed by the n-type hydrogenated nanocrystalline silicon oxide (nc-SiO_X: H) and p-type a-Si: H films. Transparent conductive oxide films were deposited using the physical vapor deposition (PVD) technology. Finally, the metallization was carried out through screen-printing processes using the low-temperature silver pastes.

2.2. Characterization

A field-emission scanning electron microscope (SEM, Zeiss Ultra Plus, Germany) was used to observe the surface morphology and vertical thickness of the silicon wafers. The silicon wafers were characterized by X-ray diffraction (XRD, D8 ADVANCE Da Vinci, Bruker). A precise electronic balance (JJ224BC, China) with an accuracy of 0.1 mg was used to measure the weights of the silicon wafers. The diffusion depth of the P/O/Si elements was observed using a time-of-flight secondary ion mass spectrometer (ION TOF ToF SIMS 5–100, Germany). The elemental contents of the substrate were measured using a wavelength dispersive X-ray fluorescence spectrometer (XRF, S8 Tiger II, Germany). PL mappings of the silicon substrate were acquired via an offline PL&EL tester (VS-6841D, China). A Time-Resolved Fluorescence Spectrofluorometer (FLS1000, UK) with a 532 nm pulsed laser source was used to detect the TRPL decay. The square resistance of the substrate was measured using a double electrodynamic four-probe tester (RTS-5, China). All of the above characterizations were for silicon wafers with or without PDG. Quasi steady state photoconductance (QSSPC) lifetime and SunsVoc were carried out using a dual-use equipment (WCT-120, Sinton, USA). EQE spectra were collected in the 300–1180 nm wavelength range using the Quantum Efficiency Measurements system (PVE300-IVT210, Bentham). Finally, Vision VS-6831S (AAA level) tested the I-V parameters in air under standard simulated AM 1.5G sunlight irradiance.

2.3. Simulations

Using Quokka 2 software, we simulated the effect of the PDG process on the electrical properties of SHJ solar cells and extracted Free Energy Loss Analysis (FELA) to understand the recombination and resistive losses [37]. Changes in pre-passivation dark saturation current density (J_0), substrate thickness, effective minority lifetime, and series resistance of the external circuit represent the effect of different PDG processes on electrical performance in the simulation software. Files generated optically were extracted from an online simulation platform (OPAL 2) [38]. The main input parameters were in the Quokka 2

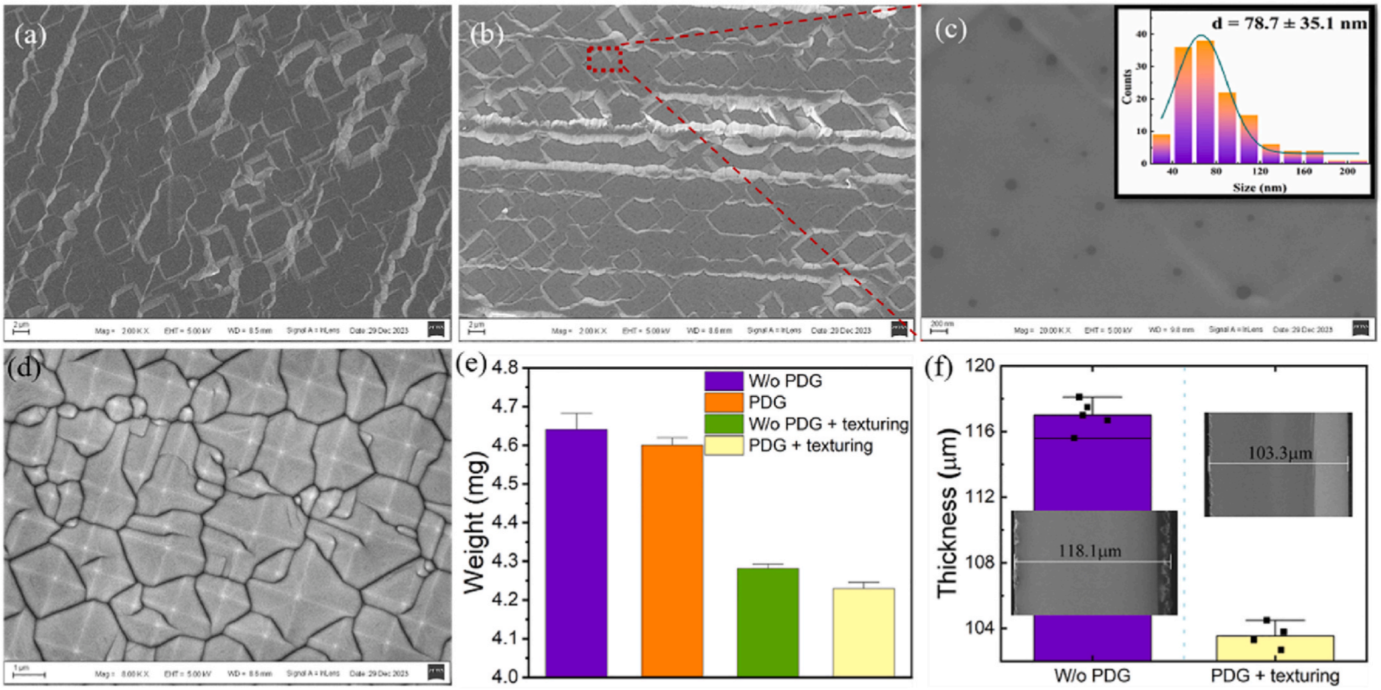

Fig. 2. Surface morphology of silicon wafers (a) without and (b) with PDG, (c) Local magnification of Fig. 2(b), and the inset in the upper right corner is the size distribution statistic of P-channels, (d) Surface pyramid morphology of silicon wafers after cleaning and texturing, (e) Influence of the PDG and texturing on the weight of the wafers, and (f) Thickness changes of the silicon wafers without and with PDG + texturing treatment. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

simulations listed in Table S1.

3. Results and discussion

Fig. 2a illustrates the surface morphology of a bare monocrystalline silicon wafer, which is obtained by cutting with diamond wires. The cutting process formed bifacial damage layer on the silicon surface, resulting in the destruction of the lattice. Chemical equations (1) and (2) describe the chemical reactions in the PDG process. For ease of use and storage, liquid phosphorus trichloride ($POCl_3$) is commonly employed as a phosphorus source carried by N_2 to the reaction chamber, decomposed into phosphorus pentoxide (P_2O_5) and phosphorus pentachloride (PCl_5) under high temperature. PCl_5 can be further decomposed into P_2O_5 and Cl_2 in sufficient O_2 conditions. The generated P_2O_5 react with Si to form a phosphorus-silicon glass (PSG) layer to complete P diffusion.

$$POCl_3 + O_2 \rightarrow 2P_2O_5 + 6Cl_2 \tag{1}$$

$$2P_2O_5 + 5Si \rightarrow 5SiO_2 + 4P \tag{2}$$

It can be seen in Fig. 2b, the PDG treatment does not influence the morphology of the damage layer, but brings a large number of holes on the surface with sizes in the range of 20–220 nm. It is evident that these holes function as channels for phosphorus diffusion into the wafers. Fig. 2c provides a magnified view and statistical distribution of the size of P channels counted to be 78.7 ± 35.1 nm.

After PDG, the silicon wafers were cleaned and textured with the strong alkali solution to obtain the bifacial micrometer-scale pyramids as shown in Fig. 2d. We have counted the change in the weight of the silicon substrate during PDG and texturing processes in Fig. 2e. The average weight of the bare wafer was 4.64 mg, and reduced to 4.60 mg after PDG. After cleaning and texturing, the weights without and with PDG treatment were 4.25 mg and 4.21 mg, respectively. Meanwhile, silicon wafers were thinned from 117 μm to 104 μm after PDG and texturing, with the corresponding representative SEM images inserted in Fig. 2f.

Fig. 3a presents a comparison of X-ray fluorescence (XRF) results for silicon wafers with and without PDG. Diffused layers after PDG were etched off before XRF measurements. The detailed content of the six major elements and the lowest limit of detection (LLD) are recorded in Table S2 and Fig. S1. The PDG process causes a 1.18 % decrease in elemental Si and a 1.31 % increase in elemental O, as indicated by equation (2). The purity of substrate is less than 99.9 % because of the used n-type wafers rather than the intrinsic wafers. The effectiveness of PDG was confirmed by successfully removing Fe, given that Fe is a known primary factor contributing to recombination losses in solar cells [11]. However, the PDG process introduced Cu from wire cutting chips or wafer carriers, causing its concentration to increase by an order of magnitude. Another possible source is residual Cu left on the wafer surface after diamond wire cutting. In contrast to Fe, the diffusion behavior of Cu may be different, which may lead to its accumulation near the surface or in the unetched area. Metallic impurities adhered to the silicon wafer may have been incorporated into the substrate during the gettering process, leading to an increase in copper content. Even the extant Cu content is not very high (238 ppm), but trace amounts of Cu can lead to photodegradation [39]. Likewise, the Pt content has increased (Table S2). P content in the substrate is below the LLD of 56.1 ppm even after P diffusion.

As shown in Fig. 3b, X-ray diffraction (XRD) indicates that the diffraction peaks of the n-type monocrystalline silicon wafers are located near 69.2° corresponding to the (100) crystal plane (JCDS #27–1403), while the diffraction peaks cleaved at 69.4° are from P-doped Si [40]. Interestingly, the characteristic peaks are shifted to a larger side by about 0.1° in the PDG treated sample, but return to the original positions after cleaning and texturing (i.e., eliminating the P-doped layer). Importantly, the peak shift is primarily attributed to O doping rather than P doping [41] according to Bragg's equation, since the O atom radius (74 p.m.) is much smaller than that of the Si atom (110 p.m.).

Due to the limitations of XRF in characterizing changes in P, we utilized time-of-flight secondary ion mass spectrometry (TOF-SIMS) to investigate the elemental distributions on the wafer surface. Fig. 4a

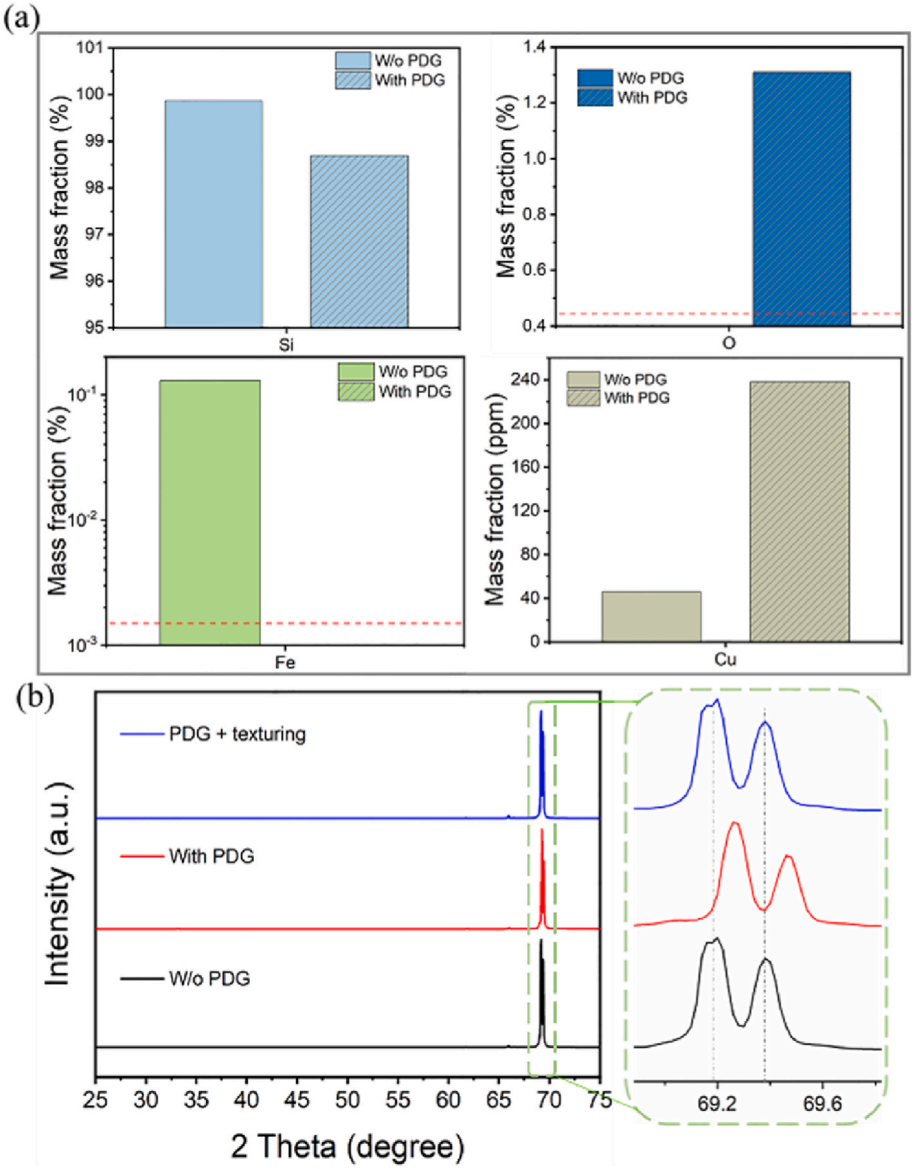

Fig. 3. (a) Changes in elemental content of silicon wafers before and after PDG, including Si, O, Fe, and Cu; the red dotted line is the lowest limit of detection (LLD). (b) X-ray diffraction (XRD) patterns of silicon wafers without PDG, with PDG and PDG + texturing. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

exhibits 3D ion distributions on the wafer surface after PDG at a depth of 300 nm. Both O^- and P^- exhibit a heavily doped layer on the surface with a thickness of about 20 nm, after which the concentration decays rapidly. To assess P diffusion, the intensity of the P^- signal is crucial. However, the intensity of PO_2^- is much higher than that of P^-, which implies that a large amount of P_2O_5 diffused into the silicon substrate is not converted into P. Vertical red bands are clearly presented from the Z-axis distribution to highlight diffuse pathways in the wafer, as depicted in both the Si^- and Total images. While these striped structures disappear from the Si^- and Total distributions after texturing in Fig. 4b, indicating that the PSG layer is essentially removed. In addition, compared to samples without PDG, the concentrations of O^- and SiO_2^- in the textured wafers significantly increased, suggesting the introduction of a new SiO_2 layer on the textured wafer surface. To enable a quantitative comparison of element diffusion depth in the wafers, distribution curves of ionic intensity with depth are plotted in Fig. 4(c and d). The slow decay of O^-, Si^- and SiO_2^- with increasing depth is mainly caused by the pyramidal structure.

Combined with equations (1) and (2), we believe that the P diffusion mainly relies on the penetration of P_2O_5 into the Si substrate. More importantly, P diffusion does not uniformly penetrate the interface but easier occurs in the form of channels. As the reaction proceeds, the product SiO_2 from P_2O_5 and Si, as well as the excess O_2 and Si, gradually segregates the contact between P_2O_5 and Si, thus preventing the reaction from continuing. Residual P^- is present on the wafer surface after texturing, possibly due to the continued reaction of remaining P_2O_5 with Si during the drying process. The process of heating and drying textured wafers lasts for 15 min at a temperature of 90 °C. During this period, compressed air is introduced into the drying tank, which may lead to surface oxidation of the silicon wafers due to the combination of 90 °C heating and air exposure.

The n-type monocrystalline wafers possess inherently a good lateral conductivity because of intrinsically being doped with P, with an average square resistance of 92.6 Ω/sq demonstrated in Fig. 5a. With ongoing P diffusion, the square resistance decreases notably to 26.5 Ω/sq at 100 sccm and 23.2 Ω/sq at 2000 sccm. To further observe the effect of PDG, we have measured the effective minority lifetime from cell precursor just before TCO deposition and saturated dark current density

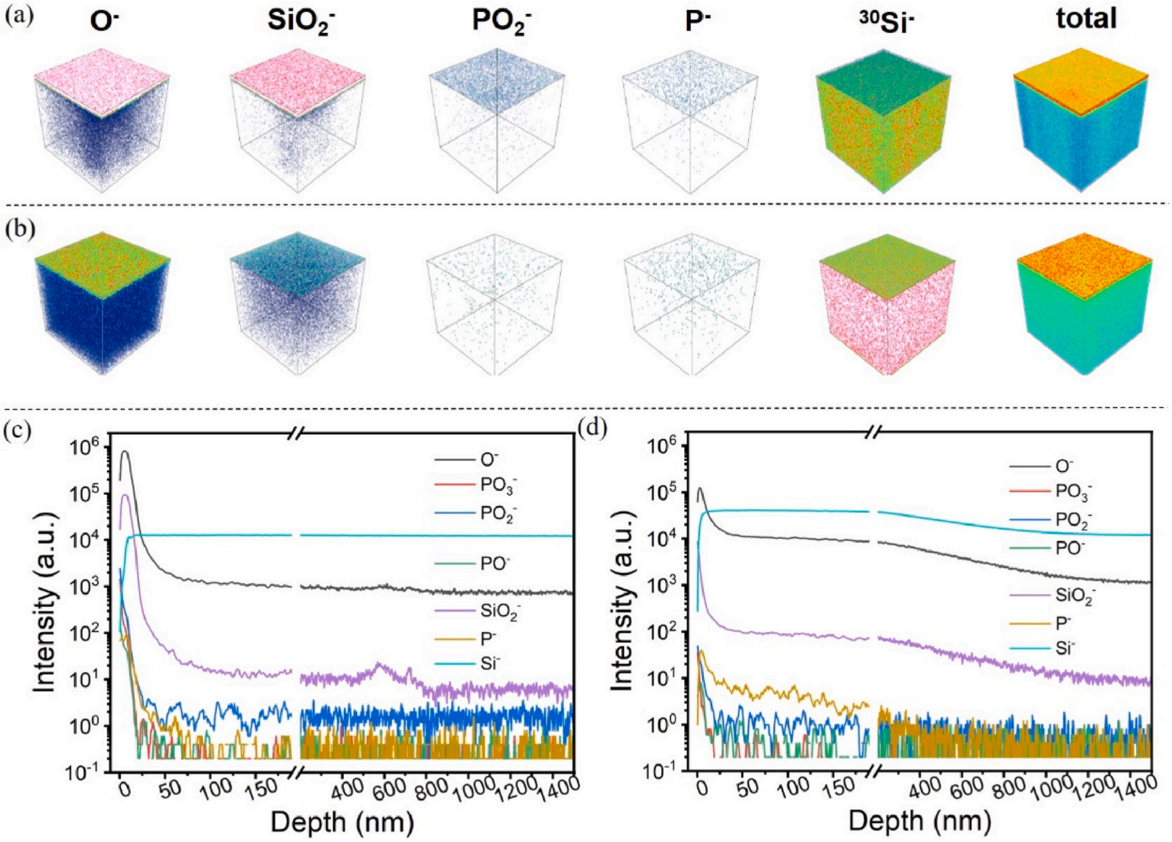

Fig. 4. Three-dimensional element distributions (O^-, SiO_2^-, PO_2^-, P^-, Si^- and total) of the silicon wafers based on TOF-SIMS with (a) PDG and (b) PDG + Texturing; TOF-SIMS curves of the silicon wafers versus depth with (c) PDG and (d) PDG + texturing. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

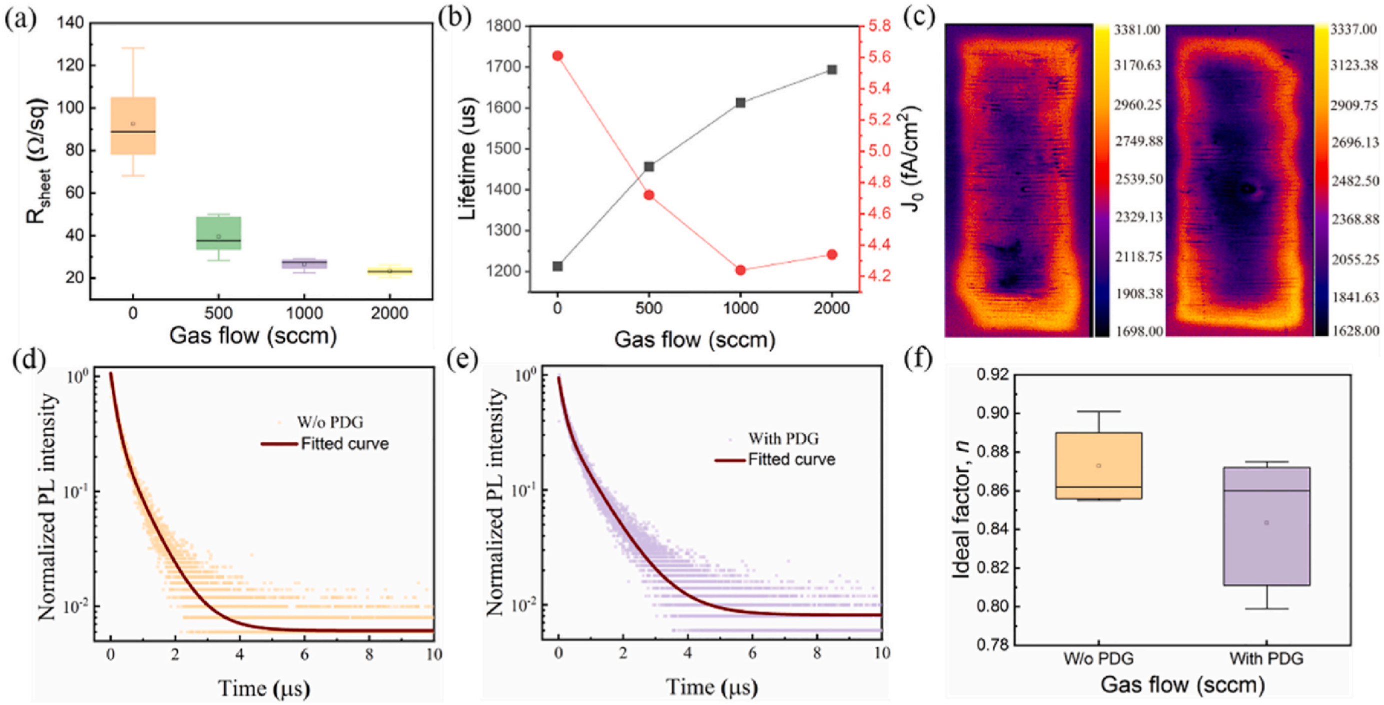

Fig. 5. (a) Square resistance, (b) effective minority lifetime (left) and saturated dark current density (right) of silicon wafers after PDG process with different gas flows. (c) PL mappings of 1000 sccm (left) and 2000 sccm (right) PDG treated silicon wafers. Time-resolved photoluminescence (TRPL) spectra based on (d) silicon wafers without and (e) with PDG process. (f) Ideal factor in high injection condition based on SHJ solar cells without and with PDG process. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

Table 1
TRPL fitting results of the textured silicon wafers without and with PDG treatment.

	τ_1 (μs)	A_1	τ_2 (μs)	A_2	τ_{avg} (μs)
W/o PDG + texturing	0.167	0.723	0.687	0.328	0.506
With PDG + texturing	0.166	0.544	0.876	0.388	0.727

(J_0) of SHJ solar cell, as depicted in Fig. 5b. As the gas flow was increased from 0 sccm to 2000 sccm, the lifetime was gradually increased from 1213 μs to 1694 μs. J_0 shows a different trend, reaching a minimum of 4.24 fA/cm^2 at a flow of 1000 sccm, whereas J_0 instead increases to 4.34 fA/cm^2 at 2000 sccm. To elucidate this phenomenon, the photoluminescence (PL) mappings in Fig. 5c are provided based on the 1000 sccm and 2000 sccm treatments. After PDG treatment, the PL intensity is significantly increased mainly at the half-edge position rather than the middle and edge position. The central region consistently shows weaker PL signals due to relatively weaker phosphorus diffusion compared to the half-edge, where direct gas contact is greater. Upon increasing the flow rate from 1000 sccm to 2000 sccm, the PL intensity in the center region of the wafer decreased. This is attributed to the higher flow rate failing to enhance the gettering effect while introducing additional impurity defects.

Time-resolved photoluminescence (TRPL) decay is further used to analyze carrier lifetime, which are typically fitted with a double exponential function as equation (3).

$$I_t = I_0 + A_1 e^{-t/\tau_1} + A_2 e^{-t/\tau_2} \tag{3}$$

And the average carrier lifetime (τ_{avg}) can be calculated from equation (4).

$$\tau_{avg} = \left(A_1\tau_1^2 + A_2\tau_2^2\right) / \left(A_1\tau_1 + A_2\tau_2\right) \tag{4}$$

Where τ_1 represents the carrier capture due to surface defects, while τ_2 reflects the carrier lifetime limited by bulk defects, respectively [42,43]. The TRPL fitting results derived from Fig. 5d-e in Table 1 indicate that τ_{avg} of the wafer is enhanced from 0.506 μs (0 sccm) to 0.727 μs (1000 sccm) after PDG, mainly due to the optimization of bulk recombination. Moreover, the ideal factor (n) of SHJ solar cell decreases from 0.875 to 0.842 due to PDG treatment, as shown in Fig. 5e. The ideal factors of Shockley-Read-Hall (SRH) recombination and Auger recombination for

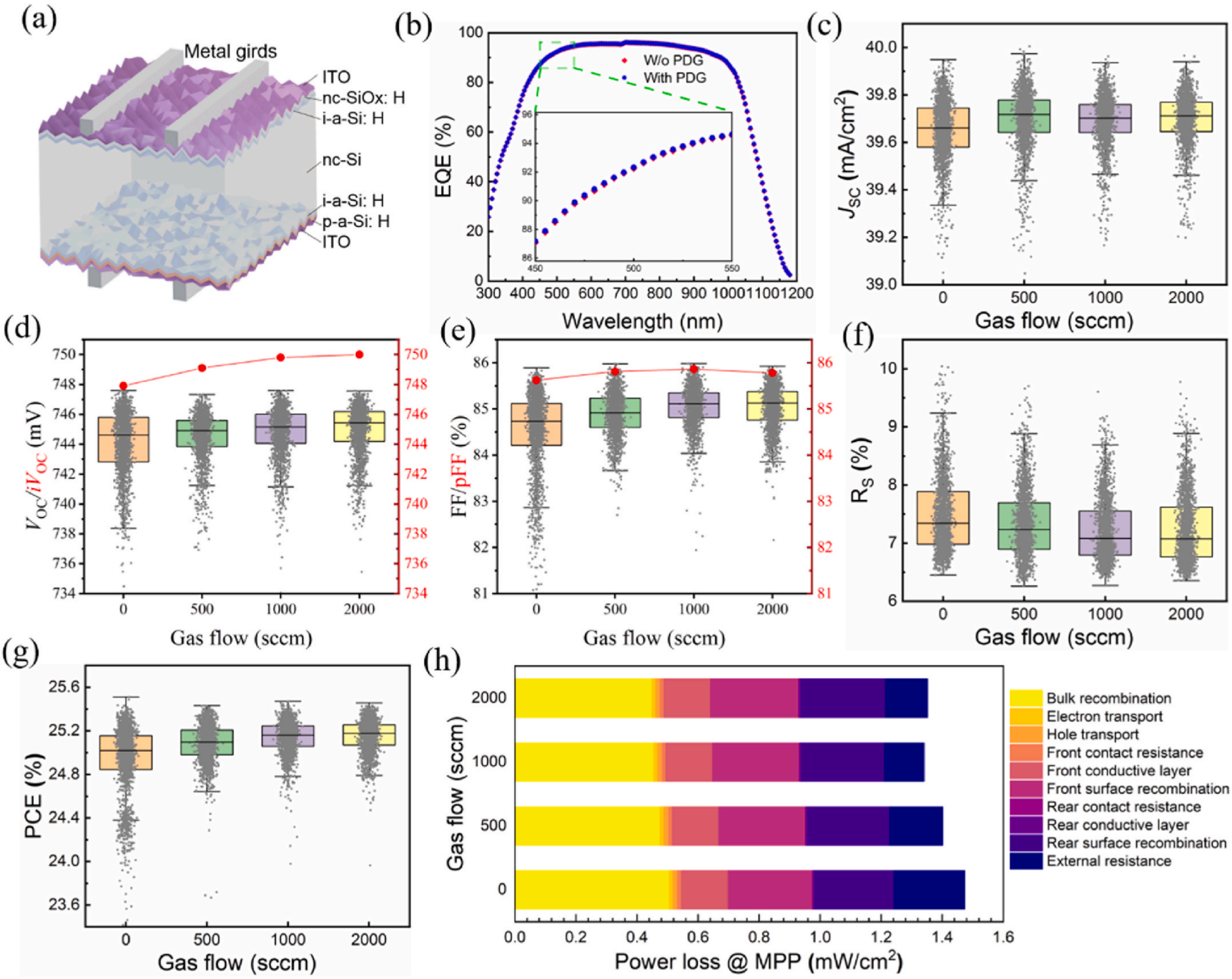

Fig. 6. (a) Schematic structure of the SHJ solar cell. (b) EQE curves of the SHJ solar cell without and with PDG. Measured photovoltaic parameters of the SHJ solar cells with different gas flows, including (c) J_{SC}, (d) V_{OC}/iV_{OC},(e) FF/pFF, (f) R_S and (g) PCE. (h) Free energy loss analysis (FELA) in SHJ solar cells with different gas flows. iV_{OC} and/pFF are red scattered points, corresponding to the right coordinate axis. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

Table 2
Photovoltaic performance of PDG processed SHJ solar cell with different gas flow.

Gas flow (sccm)	J_{SC} (mA/cm^2)	V_{OC} (mV)	FF (%)	PCE (%)	R_S (mΩ)
0	39.65	744.1	84.51	24.93	7.49
500	39.68	744.5	84.82	25.06	7.33
1000	39.69	744.8	85.04	25.14	7.22
2000	39.70	745.0	85.03	25.15	7.24

high injection conditions equal to 2 and 2/3, respectively, [44]. Increasing τ_{avg} by the PDG treatment represents a decline in SRH recombination and surface recombination, thereby reducing the ideal factor. When the loss of device is dominated Auger recombination [45], P residue after texturing interferes with Auger recombination, resulting in a deterioration of the homogeneity of the ideal factor.

To evaluate the impact of the PDG process on devices, SHJ solar cells were prepared with varying $POCl_3$ flows (>1800 samples per group), following the structure illustrated in Fig. 6a. The *J-V* parameters of the devices are summarized in Table 2. The data represent averaged values derived from over 1800 samples per group, with efficiency values corresponding to cells with average performance within each group. The corresponding external quantum efficiencies (EQE) of the SHJ solar cell without and with PDG treatment are given in Fig. 6b. The EQE values get slightly improvement after the PDG treatment, as seen in the local zoomed-in view. As shown in Fig. 6c, the short-circuit current density (J_{SC}) of the device without PDG process (0 sccm) reaches 39.65 mA/cm^2. In contrast, the PDG process with 500/1000/2000 sccm leads to an average J_{SC} enhancement of 0.03/0.04/0.05 mA/cm2, respectively. These results align with the EQE fitted J_{SC} [46]. PDG process shows a mild optical enhancement, attributed to the competing effects of improving Fe impurity removal and introducing other impurities.

In Fig. 6d, the PDG treatment results in an improvement in the open-circuit voltage (V_{OC}), which increases from 744.1 mV to 744.5, 744.8, and 745.0 mV, respectively, exhibiting a similar trend to the implied open-circuit voltage (iV_{OC}) results. The improvement in the V_{OC} originates from the enhancement of the effective minority lifetime and the reduction of J_0. Meanwhile, the fill factor (FF) of the SHJ solar cell is improved by the PDG treatment, which is shown in Fig. 6e–be 0.53 % for 1000 sccm but 0.52 % for 2000 sccm. The contribution of 2000 sccm to the FF is even slightly lower than that of 1000 sccm, which is corroborated by the pseudo-filling factor (pFF). The change in FF is related to the increase in series resistance (Rs). Hence, Fig. 6f reveals that the gas flow of 1000 sccm and 2000 sccm decrease Rs by 0.27 mΩ and 0.25 mΩ due to the decrease in bulk resistance.

Based on the J_{SC}, V_{OC} and FF results, the average PCE is improved by 0.13 %, 0.22 %, and 0.23 % due to PDG treatment in Fig. 6g, compared to the samples without PDG. The contributions in PCE and homogeneity are primarily attributed to FF. Fig. 6h reveals the simulation results of the free energy loss analysis (FELA). Significant changes in bulk recombination and external series resistance can be observed. When the gas flow rises from 0 to 2000 sccm, the power loss of the bulk recombination gradually decreases from 0.506 mW/cm^2 to 0.449 mW/cm^2. While the loss of the external resistance achieves a minimum of 0.129 mW/cm^2 at 1000 sccm. Consequently, we recommend the PDG process with 1000 sccm for SHJ solar cell. Fig. S2 provides representative *J-V* and *P-V* curves of the SHJ solar cell treated with 1000 sccm, achieving an average conversion efficiency of 25.14 % and a power output of 4.17 W.

4. Conclusions

In summary, we have performed both experimental and theoretical investigations on the application of the PDG process to n-type SHJ solar cells. We found that P diffuses deep into the silicon wafer in the form of circular channels with an average diameter of 78.7 nm. Heavily diffusion of P to a depth of about 20 nm produces an excellent uptake of Fe while inevitably introducing other impurities. A gas flow of 1000 sccm is preferred through a combination of square resistance, effective minority lifetime and J_0. The PDG treatment significantly reduced bulk recombination while surface recombination remained largely unchanged, resulting in an increase in τ_{avg} from 0.506 μs to 0.727 μs and a decrease in the ideality factor from 0.875 to 0.842. We successfully fabricated industrial SHJ solar cells (182 mm × 91 mm) with various PDG flow treatments, achieving a PCE improvement of over 0.2 % on a base value of 24.93 %, compared to devices without PDG treatment. PCE gains was derived from J_{SC}, V_{OC} and FF, with the majority of the gains stemming from FF.

Our research proves that the further optimized gettering process is very effective for the production of low-cost silicon solar cells with reducing the dependence on high-purity wafers. The potential for higher yields and improved cell efficiency further justifies the investment in PDG equipment and operational costs.

CRediT authorship contribution statement

Huanpei Huang: Writing – review & editing, Writing – original draft, Data curation, Conceptualization. **Daxue Du:** Writing – review & editing, Writing – original draft, Data curation, Conceptualization. **Lin Li:** Data curation. **Chao Gao:** Data curation. **Sheng Ma:** Data curation. **Xingbing Li:** Methodology. **Li He:** Formal analysis. **Hongzhen Su:** Formal analysis. **Dong Ding:** Formal analysis. **Zhengping Li:** Formal analysis. **Wenbin Zhang:** Methodology. **Wenzhong Shen:** Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.solmat.2024.113392.

Data availability

Data will be made available on request.

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